Kenwood TS-940 Assembly Errors

Debunking a Myth

by Dave Phillips, KB7JS

Owners of the venerable Kenwood TS-940 transceiver are often motivated to go searching for enhancement modifications for their trusty radios. If you are one of these individuals, you will find many very useful modifications that may offer some unique improvements in operability, and several upgrades that will greatly enhance and extend the service life of your radio.

However, along the way, you may encounter considerable dialog regarding supposed factory assembly mistakes, specifically with respect to incorrectly installed transistors in the RF and IF Unit.

Beware of the Soothsayers

The "Problem" to be resolved by this modification does not exist, and all of the documentation asserting it, including some very misguided comments by myself over the last few years, is technical nonsense resulting from our peers hubris and lack of understanding of the finer points of RF circuit design.

This long chain of misinformation apparently first came to life in Kenwood service bulletin that identified a manufacturing error. However, that service bulletin was quickly rescinded after the Kenwood engineers corrected the false assumption. However, the proverbial cat was "out of the bag" and like a bad joke, survives with its many repetitions intact.

An example is the following article published on the *Radiomods* website.

https://www.radiomods.co.nz/kenwood/kenwoodts940assemblyerror.html

This analysis and the suggested modification to correct the "Problem" has been widely replicated in many posts and mods articles published on-line. It is fundamentally based in the belief that specific transistors were incorrectly inserted on the RF and IF Units of the TS-940 during manufacturing at the Kenwood Factory.

While there is some history of numerous problems associated with the manual assembly of circuit boards in Kenwood radios of the 1960s – 1980s, especially the TS-930 and TS-940, almost all were the result of less than perfect soldering skills. The reality is that every assembly line suffers from Monday morning and Friday afternoon distractions.

That is not the case here, this modification is based on gross misunderstanding, and I am publishing this missive in an attempt to "Clear the Air" and stop the unnecessary mangling of fine radios.

How did this happen?

The original analysis was based on some mistaken interpretation of schematics and board layout diagrams. This resulted in the determination Kenwood had committed a serious error in the board level silkscreen masks identifying component orientation, which then resulted in the two pairs of FETs being installed incorrectly by the Kenwood personnel on the factory assembly line.

As a result of this erroneous technical assumption, many Amateur Technicians have continued to follow them and “correct” what they have been told is an error, then repeat it by further documenting it for the benefit of the Amateur Radio community et-al. Like a good or bad joke, it took on a life of its own complete with several embellishments.

Some On-line posts even claim the suggested modification resulted in a dramatic improvement in sensitivity. That assertion is patently not true, real measurements show that the modification may produce a nominal increase in gain of the stage at a narrow band of frequencies, but it is irrelevant due to the inherent loss effects of following stages, and it also results in a marked reduction in bandwidth and stability.

Good Engineering requires research

A bit of diligent research and detailed analysis of the electrical properties of both circuits reveals that the Kenwood engineers were meticulous in their design and far more competent than we mere mortals have given them credit for.

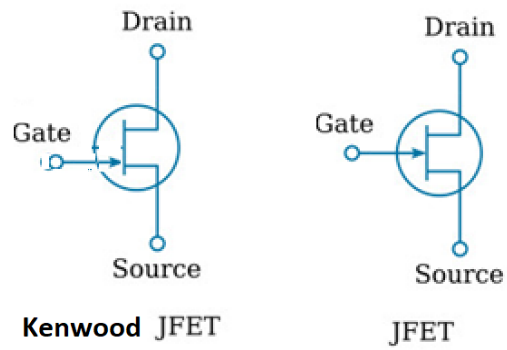
The orientation of the transistors is intentional, the circuit designs are brilliant.

Why does it work at all?

The transistors in both circuits are JFETS, a type of transistor that is physically symmetrical, the Source and Drain terminals are basically interchangeable, allowing this type to be easily adopted in place of traditional BJT’s in many common circuit applications such as buffer or switch.

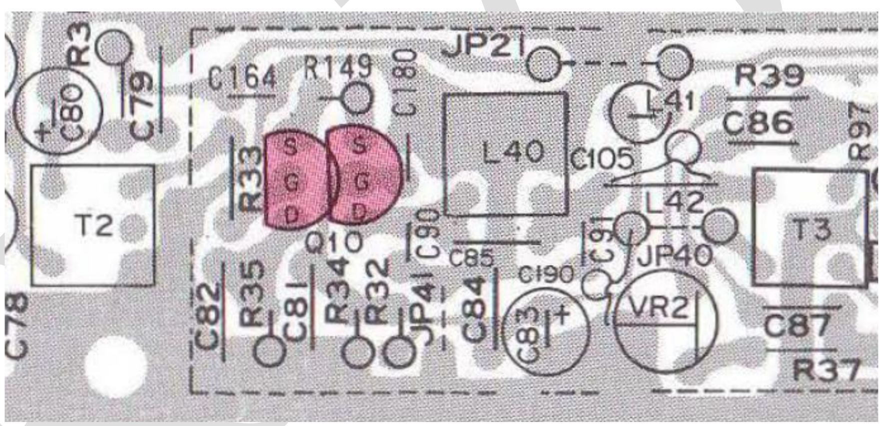
However, when used as a gain stage, there are subtle differences in how a JFET responds to stimulation as input/output capacitance can vary widely over signal frequency range. The Kenwood engineers took advantage of the subtle differences exhibited by the Drain and Source to mitigate the effects of this behavior.

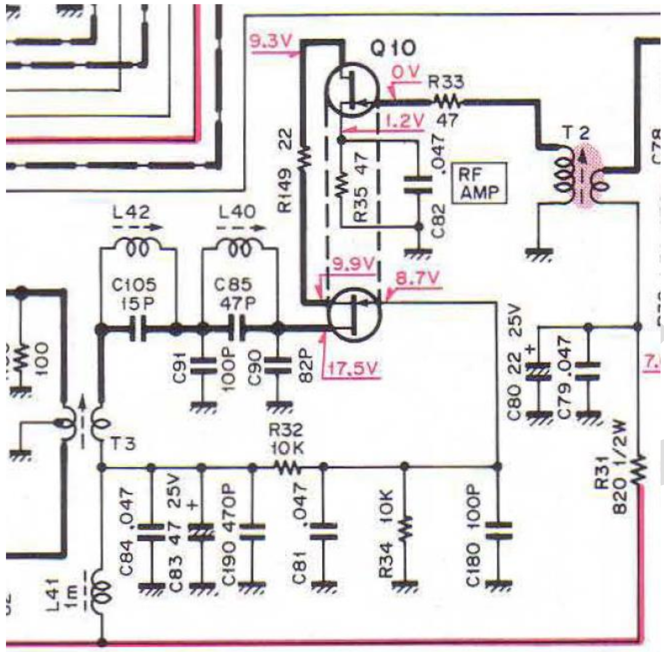
Assumptions based on the interpretation of the Kenwood schematic symbology for JFETs is precisely why these circuits have been the subject of confusion and debate for many years. The Kenwood conventional symbology for the N-Channel JFET shows the Gate terminal as a pointer offset from center, and everyone “assumes” the opposing terminal is the Source terminal. This Japanese convention was adopted as a simple method to illustrate the use of a FET in the same manner as a conventional BJT. However, that is misleading, and in this case, incorrect. Note that the conventional symbology for the JFET shows the symmetrical nature with Gate terminal centered in the symbol.



RF Unit

First, let's look at the 1st Rx Amplifier in the RF Unit, a pair of two 2SK125 FETs identified as a single component, Q10.





Technicians who have supported the need to swap these transistors assert that the board layout is wrong because it illustrates the JFETs installed with their Source terminals connected in parallel via R149. They believe that the schematic shows a more conventional arrangement with the Drain of the first transistor feeding the Source of the second, utilizing a fixed bias on its Source via R35. They assert that this would be the proper alignment of the transistors and the result would be greater gain. This assumption is incorrect. That configuration would actually be two FETs in series, two separate stages.

That is not how this circuit is designed.

Kenwood engineers designed this circuit the way the board layout shows to achieve optimal low noise performance and optimal broadband performance at RF frequencies. The circuit implementation is a dual FET amplifier employing a pair of JFETs with a common source configuration. The designation of this pair of transistors as a single element, Q10, indicates this is a ***Cascode*** implementation.

Technical Definition:

> *The **Cascode** is a two-stage amplifier that consists of a common emitter stage feeding into a common base stage when using bipolar junction transistors (BJTs)[1][2] or **alternatively a common source stage feeding a common gate stage when using field-effect transistors (FETs).***
>
> *Because there is no direct coupling from the output to input, the Miller effect is eliminated, contributing to a much higher bandwidth. Compared to a single amplifier stage, this combination may have one or more of the following characteristics: higher input–output isolation, higher input impedance, high output impedance, and greater bandwidth.*

While it is true that the output from the Drain terminal may provide slightly more voltage gain when a JFET is used as a gain stage, the Miller effect occurs as the capacitance (or impedance) between the input and output of an inverting amplifier appears much larger at the input, effectively increasing the input capacitance and reducing the amplifier's bandwidth. This variable difference in the C_{gs} and C_{ds} properties results in feedback, which then results in variable impedances at the input. As the gain increases, this effect becomes more critical, inducing parasitic noise.

The implementation of Q10 as a Cascode pair is important to circuit performance. Since there is no direct coupling of Input to Output, the Cascode design improves input-output isolation, which in turn reduces feedback. As a result, Miller effect is eliminated and bandwidth is linear. The benefit of a Cascode design is broad dynamic range and low noise, primarily because the Cascode amplifier has limited voltage gain of the first stage, which limits the change in impedance as voltage increases. Kenwood engineers chose to use the Cascode design with the Source as the output of the first stage to obtain optimum results due to its lower voltage gain.

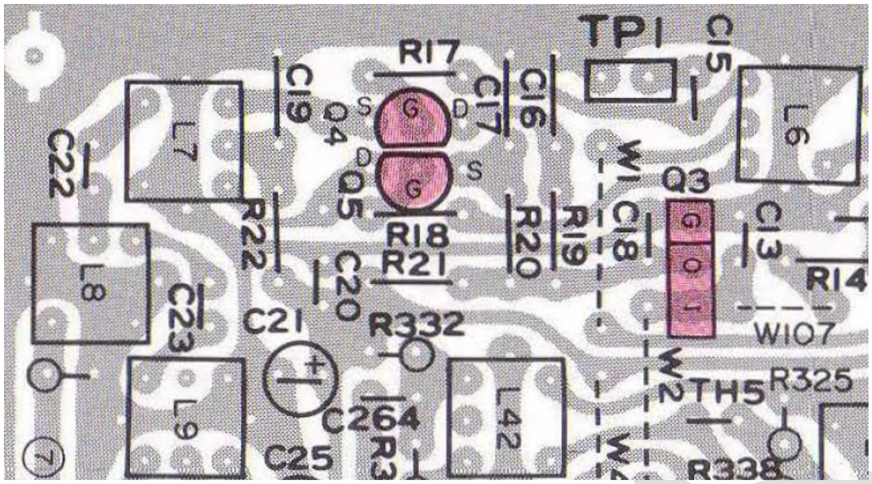
The voltage notations on the schematic for the Q10 circuit confirm that this is a Cascode design.

- The RF signal is passed through T2, a fixed biased step-up transformer. Although the schematic symbology "implies" T2 is adjustable, it is actually a simple ferrite core transformer.
- The raw RF signal from T2 is then fed to the unbiased Gate terminal of the first stage.
    - The Drain of the first stage is biased by R35 at a fixed DC voltage of +1.2V.
- The output of the first stage is taken from the Source and fed to the Source of the second stage.
- The second stage Gate is biased at a fixed +8.7V derived from the 18V rail.
- The output of the second stage is derived from its Drain terminal which is biased at 17.5V derived from the 18V rail.

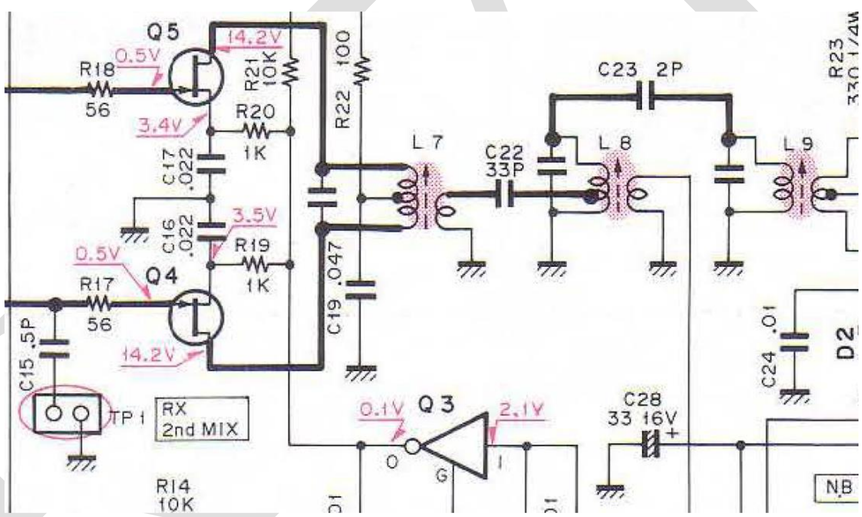
IF Unit

Now, let's look at the 2nd Rx Mixer in the IF Unit, where the same argument of "incorrectly installed" 2SK125 transistors in the 2nd RX Mixer circuit, Q4 & Q5.

Here, the transistors are installed in opposed alignment on the board layout in a stage that produces an output fed to transformer L7. Note that the circuit traces indicate that the Source of Q4 feeds on side of L7, while the Drain of Q5 feeds the other.



But the Japanese symbology on the schematic “implies” a different alignment that indicates the Drain terminals are both feeding L7 in parallel.



This stage is identified as the Rx 2nd Mixer stage that produces the 8.83MHz 2nd IF signal. However, it is important to note that the input is a Mix generated by combining the 45.05 MHz 1st IF and the 36.22 HET Oscillator is not performed in this stage, it actually occurs earlier at Transformer L6, where the mix is performed to produce a balanced feed to the Gate inputs of Q4 & Q5.

It is understandable to naturally assume that the intent of this stage is a parallel buffer amplifier with a balanced output, and that the pair of JFETs would be connected it true parallel form with using their Drain outputs. But unlike most parallel transistor amplifiers, there is no accommodation for feedback gain control.

However, when the transistors are installed as shown on the board layout, the outputs are taken from the Source of Q4 and the Drain of Q5,and this stage becomes a balanced differential amplifier.

The advantage of this implementation is high input impedance with low noise and allows the amplifier to produce balanced output signals of opposite phases (0° and 180°).

Technical Description:

> *A JFET differential amplifier, while typically used for differential-to-differential or differential-to-single-ended (drain) conversion, can be configured to take outputs from one drain and one source to provide a combination of high-gain inverting output and unity-gain non-inverting output. This configuration leverages the intrinsic property that the drain signal is 180°out of phase with the gate, while the source signal follows the gate in phase.*
>
> ***Output 1 (Drain):*** *Taken from Q4 Drain. This acts as a common-source amplifier, providing high voltage gain ($A_v \approx -\frac{g_m R_D}{2}$ $Av\approx-gmRD$/2).*
>
> ***Output 2 (Source):*** *Taken from the common Q4/Q5 Source (they are connected). This acts as a source-follower, providing a buffer with near-unity gain ($A_v \approx 1$ Av≈1) and low output impedance.*

It is very important to note that this is a balanced amplifier, with dual input and output circuit connections. Note the subtle but significant difference in the voltage notations on the fixed bias terminal of Q4 (3.4V) and Q5 (3.5V). It is easy to assume that this is simply a typographical error in the schematic, but Japanese engineers seldom make such errors. This is an effect of the common source configuration.

With the installation of the transistors as shown on the board layout, the difference in voltage gain does result in the 100 Millivolt difference. It is important to note that the 8.83 MHz input is generated by combining two signals in an adjustable impedance transformer, the 45.05 MHz RIF and the 36.22 MHz HET, and their signal levels are not balanced. Adjusting L6 for maximum output results in an average level of amplitude that favors the strongest of the two signals, the HET, so the input to Q4/Q5 will not be truly balanced. As a result, the Q4/Q5 stage is intentionally designed to act as a differential amplifier producing a balanced output. The common source configuration of the transistors ensures a stabilized balanced bipolar output.

Again, these transistors are not, and never have been, installed improperly.

Conclusion

So, if you are looking to improve or enhance the performance of your trusty Kenwood TS-940, there are many other options, but swapping the alignment of these transistors in not one of them.

73's
Dave