



SERVICE MANUAL

VHF TRANSCEIVERS

IC-F14
IC-F14S
IC-F15
IC-F15S

INTRODUCTION

This service manual describes the latest service information for the **IC-F14/IC-F14S/IC-F15/IC-F15S** VHF TRANSCEIVER at the time of publication.

MODEL	SYMBOL	CH	FREQUENCY
IC-F14	USA	16	136-174 MHz
	GEN		
IC-F14S	USA	2	
	GEN		
IC-F15	EUR	16	
IC-F15S		2	

To upgrade quality, all electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

DANGER

NEVER connect the transceiver to an AC outlet or to a DC power supply that uses more than 8 V. Such a connection could cause a fire or electric hazard.

DO NOT expose the transceiver to rain, snow or any liquids.

DO NOT reverse the polarities of the power supply when connecting the transceiver.

DO NOT apply an RF signal of more than 20 dBm (100mW) to the antenna connector. This could damage the transceiver's front end.

ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

2260002840 Switch SKHLLFA010 IC-F14 Main unit 5 pieces
8930063350 Lens 2775Lens IC-F14 Chassis 10 pieces

Addresses are provided on the inside back cover for your convenience.

REPAIR NOTES

1. Make sure the problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated turning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 30 dB to 40 dB attenuator between the transceiver and a deviation meter or spectrum analyzer when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.

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SECTION 1

SPECIFICATIONS

■ GENERAL

- Frequency coverage : 136.000–174.000 MHz
- Mode : FM
- Type of emission :

VERSION	WIDE	MIDDLE	NARROW
[USA], [GEN]	16K0F3E (25.0 kHz)	N/A	11K0F3E (12.5 kHz)
[EUR]		14K0F3E (20.0 kHz)	8K0F3E (12.5 kHz)

- Number of conventional channels : 2 ch (IC-F14S/F15S), 16 ch (IC-F14/F15)
- Antenna impedance : 50 Ω
- Operating temperature range : –30°C to +60°C (–22°F to +140°F) [USA], [GEN]
–25°C to +55°C [EUR]
- Power supply requirement : 7.2 V DC nominal (negative ground)
- Current drain (at 7.2 V DC ; approx.) :

RECEIVING		TRANSMITTING	
Stand-by	Max. audio	High (at 5 W)	Low (at 1 W)
70 mA	300 mA	1.5 A	0.7 A

- Dimensions (projections not included) : 53(W)×120(H)×38(D) mm; 2³/₃₂(W)×4²/₃₂(H)×1¹/₂(D) in
- Weight (Including BP-231) : Approximately 260 g (9³/₁₆ oz)

■ TRANSMITTER

- Output power (at 7.2 V DC) : 5 W
- Modulation : Variable reactance frequency modulation
- Maximum permissible deviation : ±5.0 kHz (Wide), ±4.0 kHz (Middle), ±2.5 kHz (Narrow)
- Frequency error : ±2.5 ppm
- Spurious emissions : 80 dB (typical) [USA], [GEN]
0.25 μW (≤ 1 GHz), 1.0 μW (> 1 GHz) [EUR]
- Adjacent channel power : 70 dB min. (Wide, Middle ; 80dB typ.)
60 dB min. (Narrow ; 70dB typ.)
- Audio harmonic distortion : 3% typical (1 kHz, 40% deviation)
- Hum and Noise ([USA], [GEN]) (without CCITT filter) : 40 dB min. (46 dB typical) for Wide
34 dB min. (40 dB typical) for Narrow
- Residual modulation ([EUR] only) (with CCITT filter) : 45 dB min. (55 dB typical) for Wide
43 dB min. (53 dB typical) for Middle
40 dB min. (50 dB typical) for Narrow
- Limiting charact of modulator : 60–100% of maximum deviation
- Microphone impedance : 2.2 kΩ

■ RECEIVER

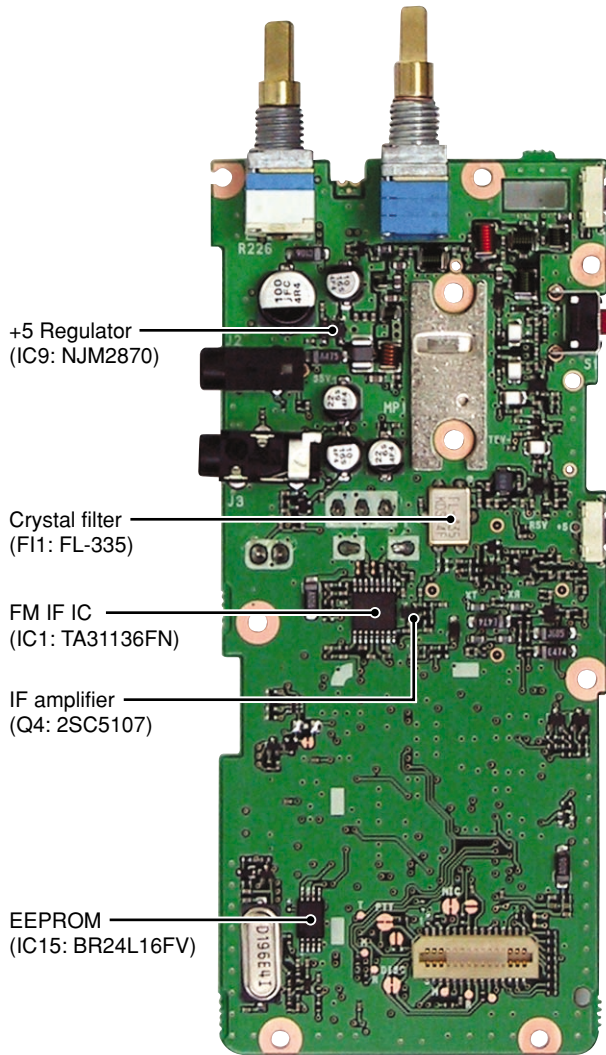
- Receive system : Double conversion superheterodyne system
- Intermediate frequencies : 1st IF: 46.35 MHz, 2nd IF: 450 kHz
- Sensitivity : 0.25 μV (–119 dBm) typical at 12 dB SINAD [USA], [GEN]
–4 dBμ (–111 dBm) emf typical at 20 dB SINAD [EUR]
- Adjacent channel selectivity : 70 dB min. (75 dB typical) for Wide and Middle
60 dB min. (65 dB typical) for Narrow
- Spurious response : 70 dB min.
- Intermodulation rejection ratio : 70 dB min. (74 dB typical) [USA], [GEN]
65 dB min. (67 dB typical) [EUR]
- Hum and Noise ([USA], [GEN] only) (without CCITT filter) : 40 dB min. (50 dB typical) for Wide
34 dB min. (45 dB typical) for Narrow
- Hum and Noise ([EUR] only) (with CCITT filter) : 45 dB min. (55 dB typical) for Wide
43 dB min. (53 dB typical) for Middle
40 dB min. (50 dB typical) for Narrow
- Audio output power : 0.5 W typical at 5% distortion with an 8 Ω load
- Squelch sensitivity (at threshold) : 0.25 μV typical [USA], [GEN]
–4 dBμV emf typical [EUR]
- Output impedance (Audio) : 8 Ω

Specifications are measured in accordance with EIA-152-C/204D, TIA-603 or EN 300 086.
All stated specifications are subject to change without notice or obligation.

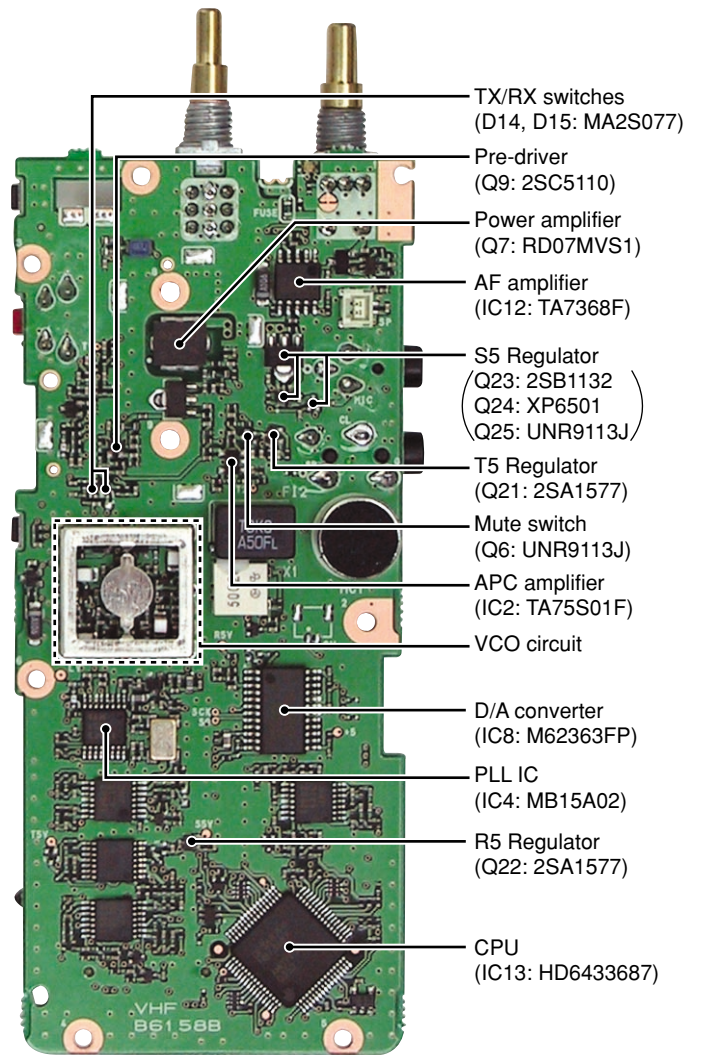
SECTION 2 INSIDE VIEWS

● MAIN UNIT

TOP VIEW



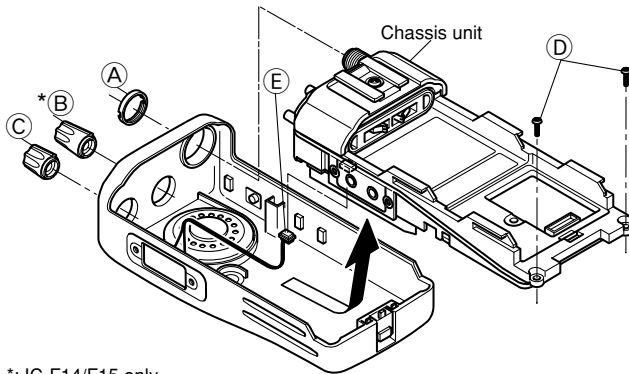
BOTTOM VIEW



SECTION 3 DISASSEMBLY INSTRUCTIONS

● REMOVING THE CHASSIS UNIT

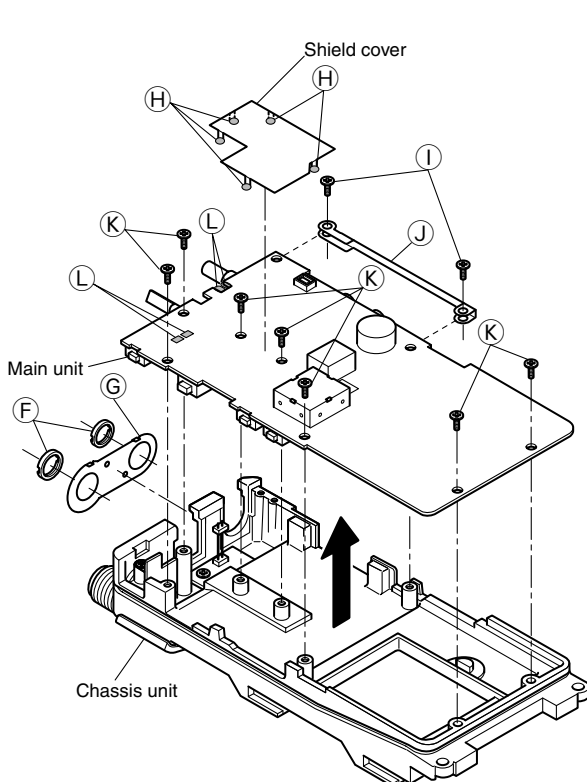
- ① Unscrew 1 nut (A), and remove 2 knobs (B), (C).
- ② Unscrew 2 screws (D).
- ③ Take off the chassis unit in the direction of the arrow.
- ④ Unplug the connector (E) from the chassis unit.



*: IC-F14/F15 only

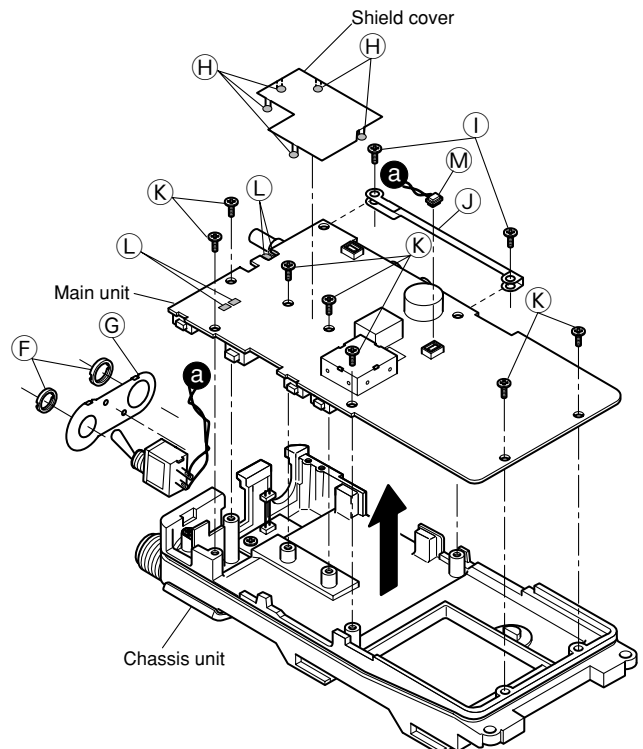
● REMOVING THE MAIN UNIT (IC-F14/F15)

- ① Unscrew 2 nuts (F), and remove the top plate (G).
- ② Unsolder 5 points (H), and remove the shield cover.
- ③ Unscrew 2 screws (I), and remove the side plate (J).
- ④ Unscrew 7 screws (K).
- ⑤ Unsolder 4 points (L), and take off the main unit in the direction of the arrow.



● REMOVING THE MAIN UNIT (IC-F14S/F15S)

- ① Remove the switch connector (M).
- ② Unscrew 2 nuts (F), and remove the top plate (G).
- ③ Unsolder 5 points (H), and remove the shield cover.
- ④ Unscrew 2 screws (I), and remove the side plate (J).
- ⑤ Unscrew 7 screws (K).
- ⑥ Unsolder 4 points (L), and take off the main unit in the direction of the arrow.



SECTION 4

CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT

The antenna switching circuit functions as a low-pass filter while receiving and a resonator circuit while transmitting. This circuit does not allow transmit signals to enter the receiver circuits.

Received signals enter the antenna connector (CHASSIS; J1) and pass through the low-pass filter (L1–L3, C2–C5, C175, C176). The filtered signals are passed through the $\frac{1}{4}\lambda$ type antenna switching circuit (D5, D6, L6, L7) and then applied to the RF circuit.

4-1-2 RF CIRCUIT

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit pass through the bandpass filter (D4, D8, L8, L9). The filtered signals are amplified at the RF amplifier (Q2) and then passed through the another bandpass filter (D9, D10, L11) to suppress unwanted signals. The filtered signals are applied to the 1st mixer circuit.

D4, D8–D10 employ varactor diodes, that are controlled by the CPU via the D/A converter (IC8), to track the bandpass filter. These varactor diodes tune the center frequency of an RF passband for wide bandwidth receiving and good image response rejection.

4-1-3 1ST MIXER AND 1ST IF CIRCUITS

The 1st mixer circuit converts the received signal into fixed frequency of the 1st IF signal with the PLL output frequency. By changing the PLL frequency, only the desired frequency passes through a crystal filter at the next stage of the 1st mixer.

The RF signals from the bandpass filter are mixed with the 1st LO signals, where come from the RX VCO circuit via the attenuator (R26–R28), at the 1st mixer circuit (Q3) to produce a 46.35 MHz 1st IF signal. The 1st IF signal is passed through a monolithic filter (F11) in order to obtain selection capability and to pass only the desired signal. The filtered signal is applied to the 2nd IF circuit after being amplified at the 1st IF amplifier (Q4).

4-1-4 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal into a 2nd IF signal. The double-conversion superheterodyne system (which convert receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

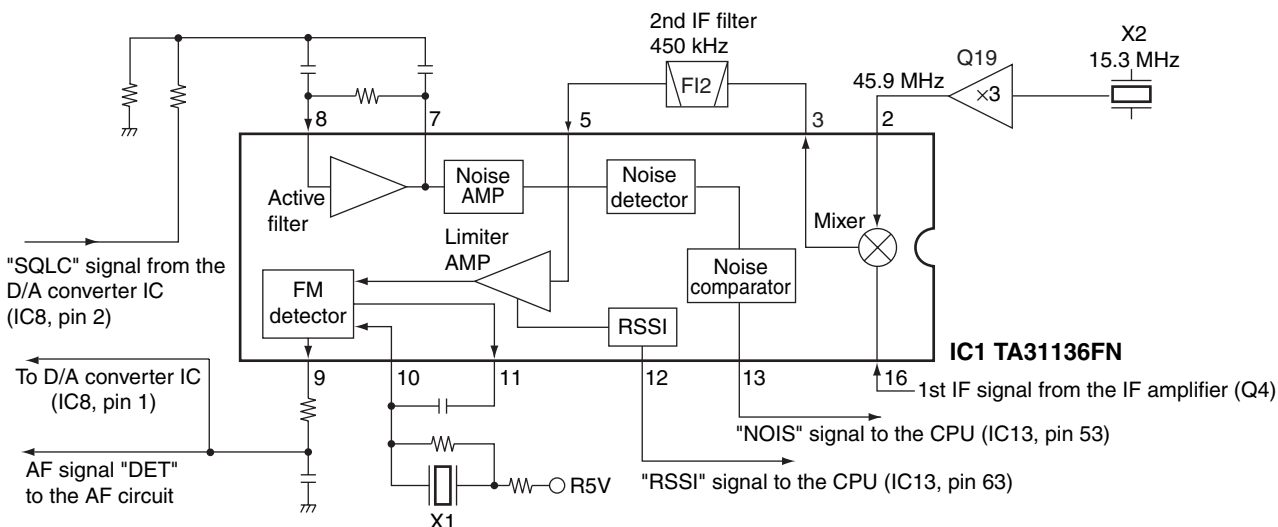
The 1st IF signal from the IF amplifier (Q4) is applied to the 2nd mixer section of the FM IF IC (IC1, pin 16), and is mixed with the 2nd LO signal to be converted into a 450 kHz 2nd IF signal.

The FM IF IC (IC1) contains the 2nd mixer, 2nd local oscillator, limiter amplifier, quadrature detector, active filter and noise amplifier circuits. A 2nd LO signal (45.9 MHz) is produced at the PLL circuit by tripling its reference frequency (15.3 MHz).

The 2nd IF signal from the 2nd mixer (IC1, pin 3) passes through the ceramic filter (F12) to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier section (IC1, pin 5) and applied to the quadrature detector section (IC1, pins 10, 11) to demodulate the 2nd IF signal into AF signals.

The demodulated AF signals are output from pin 9 (IC1) as "DET" signal, and are then applied to the AF circuit.

• 2ND IF AND DEMODULATOR CIRCUITS



4-1-5 AF AMPLIFIER CIRCUIT

The AF amplifier circuit amplifies the demodulated AF signals to drive a speaker.

The AF signals from the FM IF IC (IC1, pin 9) pass through the high-pass filter (IC6, pins 3 and 1) to suppress unwanted harmonic components. The signals pass through the RX mute switch (Q34) which is controlled by "RMUT" signal from the CPU (IC13, pin 56), and are then applied to another high-pass filter (IC6, pins 13 and 14). The filtered signals pass through the low-pass filter (IC6, pins 6 and 7) via the analog switch (IC10, pins 1 and 2). The signals are applied to the analog switch (IC10, pin 10) again, and are then applied to the AF power amplifier (IC12, pin 4) via the AF volume (R226). The amplified AF signals are output from pin 10, and are then applied to the internal speaker which is connected with J1 via the [SP] jack.

4-1-6 RECEIVE MUTE CIRCUITS

• NOISE SQUELCH

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

Some noise components in the AF signals from the FM IF IC (IC1, pin 9) are applied to the D/A converter (IC8, pin 1) as "DET" signal, and are then output from pin 2. The signals are applied to the active filter section in the FM IF IC (IC1, pin 8). The active filter section filters and amplifies noise components. The amplified signals are converted into the pulse-type signals at the noise detector section and output from pin 13 as "NOIS" signal.

The "NOIS" signal from the FM IF IC is applied to the CPU (IC13, pin 53). Then the CPU analyzes the noise condition and outputs the AF mute control signal from the CPU (pin 56) as "RMUT" signal. The signal is applied to the RX mute switch (Q34) to control the AF signal muting.

• CTCSS AND DTCS

The tone squelch circuit detects tone signals and opens the squelch only when receiving a signal containing a matched subaudible tone (CTCSS or DTCS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

A portion of the "DET" signals from the FM IF IC (IC1, pin 9) passes through the low-pass filter (IC7, pins 10 and 8) to remove AF (voice) signals, and are then applied to the amplifier (IC7, pin 12). The amplified signals are applied to the CTCSS or DTCS decoder inside of the CPU (IC13, pin 60) as the "CDEC" signal. The CPU outputs AF mute control signal, and is then applied to the RX mute switch (Q34) and analog switch (IC10, pins 12 and 13) to control AF signals muting as "RMUT" signal.

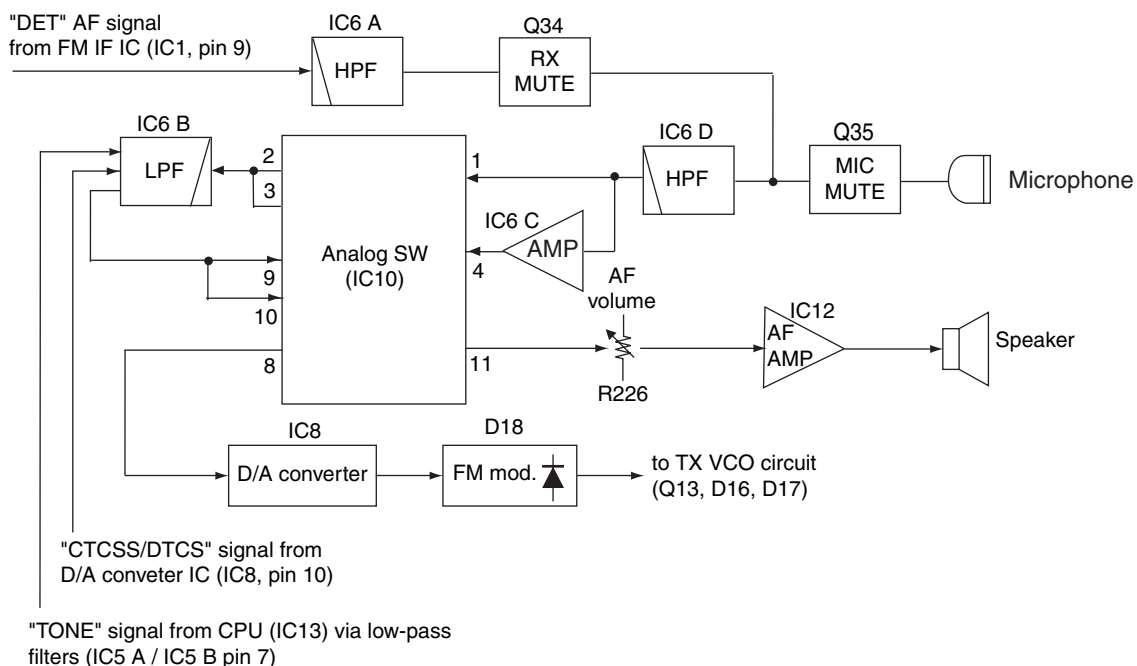
4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT

The microphone amplifier circuit amplifies audio signals within +6 dB/octave pre-emphasis characteristics from the microphone to a level needed for the modulation circuit.

The AF signals from the microphone are passed through the microphone mute switch (Q35), and are then applied to the amplifier (IC6, pins 9 and 8) via the high-pass filter (IC6, pins 13 and 14). The amplified signals are applied to the analog switch (IC10, pin 4), and outputs from pin 3. The signals pass through the low-pass filter (IC6, pins 6 and 7), then applied to the analog switch (IC10, pin 9) again. The signals are applied to the D/A converter (IC8, pin 4). The converted signals output from pin 3, and applied to the modulation circuit (D18) as "MOD" signal.

• ANALOG SWITCHING CIRCUITS



4-2-2 MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signals. The AF signals from the D/A converter (IC8, pin 3) change the reactance of varactor diode (D18) to modulate the oscillated signal at the TX VCO circuit (Q13, D16, D17). The modulated VCO signal is amplified at the buffer amplifiers (Q12, Q10) and is then applied to the drive amplifier circuit via the T/R switch (D14).

The CTCSS/DTCS signals ("CENC0", "CENC1", "CENC2") from the CPU (IC13, pins 23-25) pass through the low-pass filter (IC5, pins 12 and 14) via 3 registers (R191-R193) to change its wave form. Then the signals are applied to the D/A converter (IC8, pin 9). The output signals from the D/A converter (IC8, pin 10) pass through the low-pass filter (IC6, pins 6 and 7) to be mixed with "MOD" signal at the filter (IC6), and are then applied to the D/A converter again (IC8, pin 4).

4-2-3 DRIVE/POWER AMPLIFIER CIRCUITS

The drive/power amplifier circuits amplify the VCO oscillating signal to an output power level.

The modulated RF signal from the TX VCO circuit passes through the T/R switch (D14), and is amplified at the pre-drive (Q9), drive (Q8) and power (Q7) amplifiers to obtain 5 W of RF power (at 7.2 V DC).

The amplified signal passes through the power detector (D1), antenna switch (D2) and low-pass filter (L1-L3, C2-C5, C175, C176), and is then applied to the antenna connector (CHASSIS unit; J1).

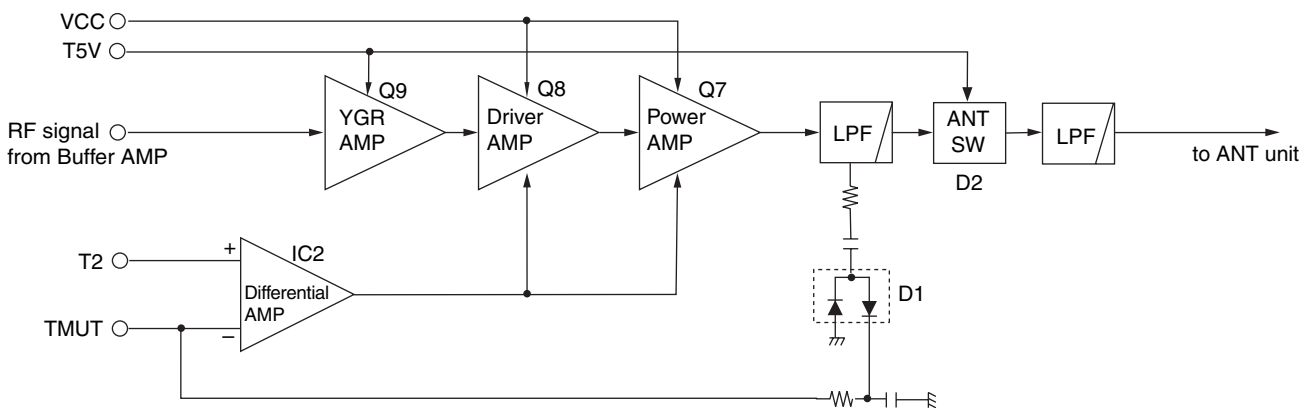
The bias current of the pre-drive (Q9), drive (Q8) and power (Q7) amplifiers are controlled by the APC circuit.

4-2-4 APC CIRCUITS

The APC circuit (IC2, D1) protects drive and power amplifiers from the reflected signal, and selects output power of HIGH, LOW2 or LOW1. The power detector (D1) detects transmit output power and converts it into DC voltage. The DC voltage is at a minimum level when the antenna impedance is matched to 50 Ω, and increased when mismatched.

The detected voltage is applied to the differential amplifier (IC2, pin 3), and the "T2" signal from the D/A converter (IC8, pin 23), controlled by the CPU (IC13), is applied to the other input for reference. When antenna impedance is mismatched, the detected voltage exceeds the power setting voltage. Then the output voltage of the differential amplifier (IC2, pin 4) controls the input current of the pre-drive (Q9), drive (Q8) and power (Q7) amplifiers to reduce the output power.

• APC CIRCUITS



4-3 PLL CIRCUITS

4-3-1 PLL CIRCUIT

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

The PLL circuit contains the TX/RX VCO circuits (TX: Q13, D16, D17, D21; RX: Q14, D19, D20, D22). The oscillated signal is amplified at the buffer amplifiers (Q11, Q12) and then applied to the PLL IC (IC4, pin 8) after being passed through the low-pass filter (L32, C206–C208).

The phase detected signal outputs from pins 15 and 16, and is then applied to the charge pump (Q39, Q40). The signal passes through the loop filter (C146, C147, C149, R95–R97), and is then applied to the TX and RX VCO circuits as a lock voltage.

The PLL IC contains a prescaler, programmable counter, programmable divider and phase detector, etc. The entered signal is divided at the prescaler and programmable counter section by the N-data ratio from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency.

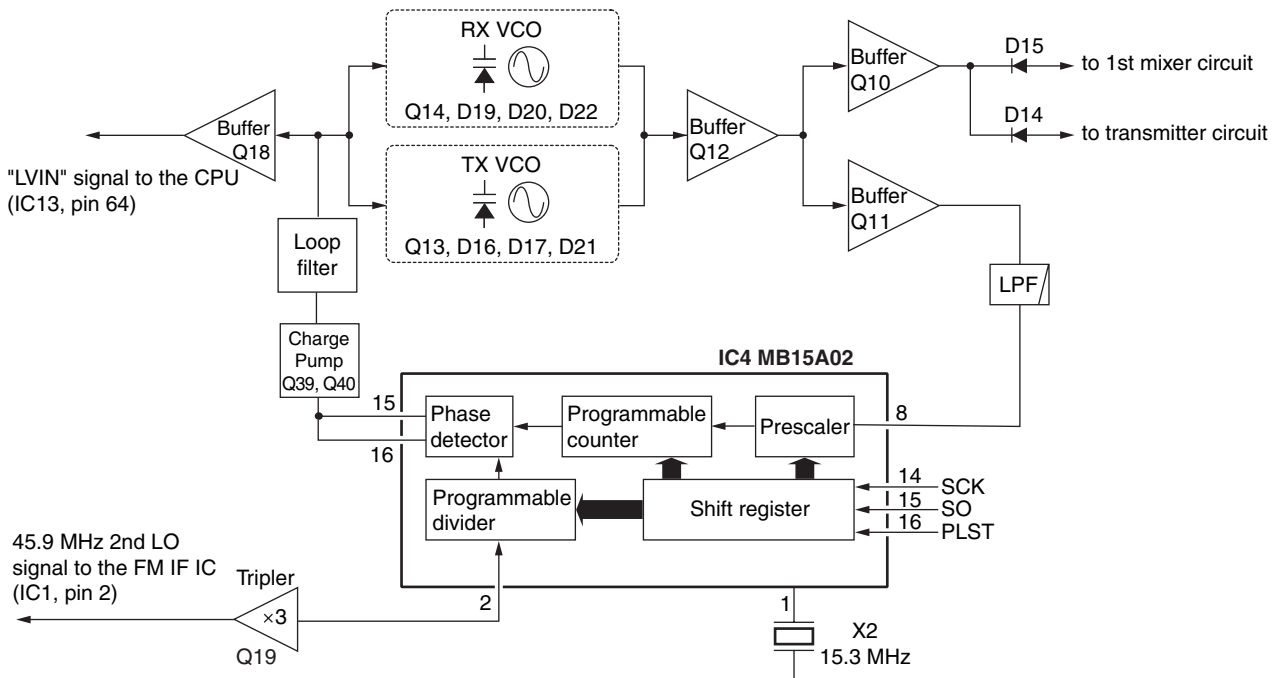
If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

4-3-2 VCO CIRCUIT

The VCO circuit contains a separate RX VCO (Q14, D19, D20) and TX VCO (Q13, D16, D17). The oscillated signal is amplified at the buffer amplifiers (Q10, Q12) and is then applied to the T/R switch (D14 for TX, D15 for RX). Then the receive 1st LO (RX) signal is applied to the 1st mixer circuit (Q3) and the transmit (TX) signal to the pre-drive amplifier (Q9).

A portion of the signal from the buffer amplifier (Q12) is fed back to the PLL IC (IC4, pin 8) via the buffer amplifier (Q11) and low-pass filter (L32, C206–C208) as the comparison signal.

PLL CIRCUITS



4-4 OTHER CIRCUITS

LED CONTROL CIRCUITS

The LED control circuit is composed of the CPU (IC13), LED driver (Q32) and LED (DS1).

The CPU outputs “RLED” and “TLED” signals from the pins 42 and 43. The signals are applied to the LED driver (Q32, pins 3 and 1). The driver outputs LED control signals to the LED (DS1).

CONDITION	COLOR
RECEIVING (2/5-TONE CODE)	ORANGE (Lighting)
LOW BATTERY (Nearly exhausted)	RED (Blinks Slowly)
LOW BATTERY (Almost exhausted)	RED (Blinks Fast)
CLONING	ORANGE (Blinking)
RECEIVING/SQUELCH OPEN	GREEN (Lighting)
TRANSMITTING	RED (Lighting)

4-5 POWER SUPPLY CIRCUIT

VOLTAGE LINE

LINE	DESCRIPTION
VCC	The voltage from the connected battery pack.
+5V	Common 5 V converted from the VCC line at the +5 regulator circuit (IC9). The output voltage is supplied to the D/A converter (IC8), analog SW (IC10) and so on.
S5V	Common 5 V converted from the VCC line at the S5 regulator circuit (Q23–Q25). The output voltage is supplied to the ripple filter (Q17), PLL IC (IC4), etc.
R5V	Receive 5 V converted from the S5V line at the R5 regulator circuit (Q22). The output voltage is supplied to the tripler (Q19), FM IF IC (IC1), IF amplifier (Q4), VCO switch (Q15, Q16), 1st mixer (Q3), etc.
T5V	Transmit 5 V converted from the S5V line at the T5 regulator circuit (Q21). The output voltage is supplied to the pre-drive (Q9), APC amplifier (IC2).

4-6 PORT ALLOCATION

4-6-1 D/A CONVERTER IC (IC8)

Pin number	Port name	Description
11	BAL	Outputs the modulation balance level control signal. The signal is applied to the buffer amplifier (IC7, pin 3).
23	T2	<ul style="list-style-type: none"> Outputs the bandpass filter tuning signal during receive. The output signal is applied to the bandpass filters (D9, D10). Outputs the TX power control signal during transmit. The output signal is applied to the APC amplifier (IC2, pin 1).
22	T1	Outputs the bandpass filter tuning signal. The output signal is applied to the bandpass filters (D4, D8).
14	LVA	Outputs the PLL lock voltage control signal. The output signal is applied to the buffer amplifier (IC7, pin 3).
15	REF	Outputs the reference oscillator correcting voltage. The voltage is applied to the buffer amplifier (IC7, pin 5).

4-6-2 CPU (IC13)

Pin number	Port name	Description
1	TEMP	Input port for the transceiver's internal temperature detecting signal.
2	BATV	Input port for the detect signal for connecting battery pack's voltage.
7	RES	Input port for power reset signal.
13	SENC0	Output single tone encoder signal.
14	SENC1	
16	DUSE	Outputs DTSC LPF control signal.
17	BUSY	
18	AFON	Outputs AF power amplifier control signal.
19	SENC2	Output single tone encoder signal.
20	SENC3	
21	CBI0	Input ports for ritary selectoir.
22	CBI1	
23	CENC0	Output CTCSS/DTCS signals.
24	CENC1	
25	CENC2	
26	CBI2	Input ports for ritary selectoir.
27	CBI3	
28	SCK	Outputs serial clock signal to the PLL IC (IC4, pin 9), D/A convertor (IC6, pin 7), etc.
29	SO	Outputs serial data to the PLL IC (IC6, pin 8) and D/A convertor (IC6, pin 8).
30	BEEP	Outputs beep audio signals.
31	ESDA	I/O port for data signals from/to the EEPROM (IC15, pin 5).
32	ESCL	Outputs clock signal to the EEPROM (IC15, pin 6).
33	UNLK	Input port for unlock signal from PLL IC.
34	PLST	Outputs strobe signals to the PLL IC (IC4, pin 11).
36	NWC	Output/input port for wide/narrow control signal.
37	DAST	<ul style="list-style-type: none"> • Outputs strobe signals to the D/A convertor (IC8, pin 6). • Input port for the connecting battery type detect signal.
38	S5C	Outputs power save control signal.
39	T5C	Outputs T5 regurator control signal. Low: While transmitting
40	R5C	Outputs R5 regurator control signal. Low: While receivinging

Pin number	Port name	Description
42	RLED	Outputs receiving LED control signal.
43	TLED	Outputs transmitting LED control signal.
44	OPT3	I/O ports for option unit.
45	OPT1	
46	OPT2	
47	PTT	Input port for the PTT switch detection signal. Low : While the PTT switch is pushed.
48	SI	Serial Bus inputport.
49	CLI	Input port for the cloning data signal.
50	CLO	Outputs the cloning data signal.
53	NOIS	Input port for the noise signal from the FM IF IC (MAIN unit; IC1, pin 13).
54	CIRQ	Input port for option unit detection.
55	CCS	Outputs chip select signal.
56	TMUT	Outputs transmit mute signal.
57	RMUT	Input port for AF mute signal from the RX circuit.
58	MMUT	Outputs MIC mute signal.
59	REMO	Inputs key signal from remote mic.
60	CDEC	Input port for CTCSS/DTCS signal from the amplifier (IC5, pin 8).
61	SDEC	Input port for single tone decode signal from the LPF (IC5, pin 8).
62	KEY	Inputs key input signal.
63	RSSI	Input port for the S-meter signal from the FM IF IC (IC1, pin 12).
64	LVIN	Input port for the PLL lock voltage.

SECTION 5 ADJUSTMENT PROCEDURES

5-1 PREPARATION

When adjusting IC-F14/S, the optional CS-F14 ADJ ADJUSTMENT SOFTWARE (Rev. 1.0 or later), JIG cable (see the illust below) and OPC-478 CLONING CABLE (RS-232 type) or OPC-478U (USB type) are required.

■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 7.2 V DC Current capacity : 5 A or more	Audio generator	Frequency range : 300–3000 Hz Output level : 1–500 mV
FM deviation meter	Frequency range : DC–300 MHz Measuring range : 0 to ±10 kHz	Attenuator	Power attenuation : 40 or 50 dB Capacity : 10 W or more
Frequency counter	Frequency range : 0.1–300 MHz Frequency accuracy : ±1 ppm or better Sensitivity : 100 mV or better	Standard signal generator (SSG)	Frequency range : 100–300 MHz Output level : 0.1 μV–32 mV (–127 to –17 dBm) (As open circuit.)
Digital multimeter	Input impedance : 10 MΩ/V DC or better	DC voltmeter	Input impedance : 50 kΩ/V DC or better
RF power meter (terminated type)	Measuring range : 1–20 W Frequency range : 100–300 MHz Impedance : 50 Ω SWR : Less than 1.2 : 1	Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–20 V
		AC millivoltmeter	Measuring range : 10 mV–10 V

■ SYSTEM REQUIREMENTS

- Microsoft® Windows® 98/SE/ME/2000/XP
- RS232C/USB port

■ BEFORE STARTING SOFTWARE ADJUSTMENT

Clone adjustment frequencies, TX power, CTCSS frequency, DTCS code and IF bandwidth (see ADJUSTMENT CONFIGURATION on the next page) into the transceiver using with the CS-F14 CLONING SOFTWARE before starting SOFTWARE ADJUSTMENTS. Otherwise, the transceiver can not be adjusted.

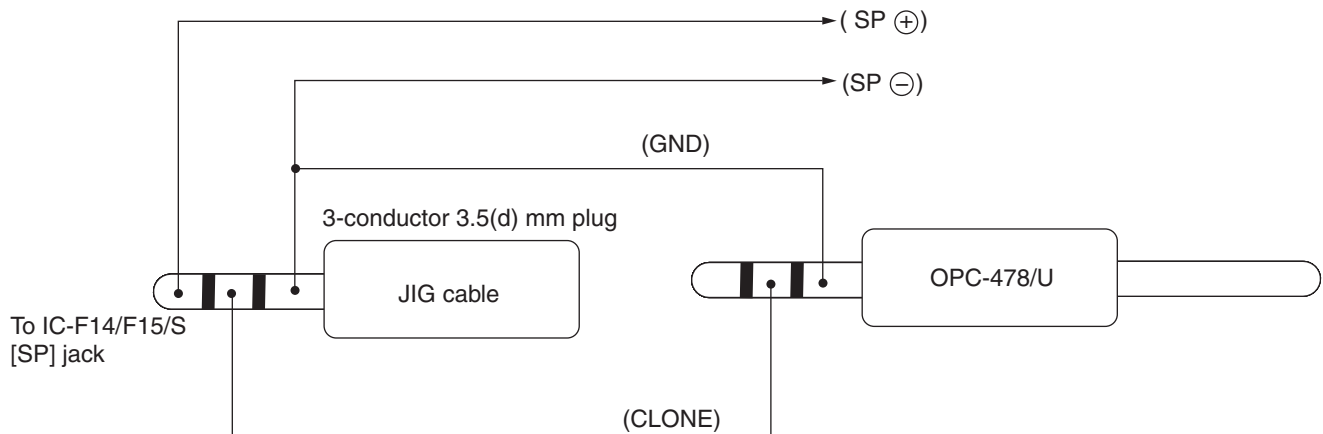
CAUTION!: BACK UP the originally programmed memory data in the transceiver before programming the adjustment frequencies. When program the adjustment frequencies into the transceiver, the transceiver's memory data will be overwritten and lose original memory data at the same time.

■ STARTING SOFTWARE ADJUSTMENT

- (1) Connect IC-F14 and PC with OPC-478/U and JIG CABLE.
- (2) Turn the transceiver power ON.
- (3) Boot up Windows, and click the program group 'CS-F14 ADJ' in the 'Programs' folder of the [Start] menu, then CS-F14 ADJ's window appears.
- (4) Click 'Connect' on the CS-F14's window, then appears IC-F14's up-to-date condition.
- (5) Set or modify adjustment data as desired.

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• JIG CABLE



5-2 CONFIGURATION LIST FOR ADJUSTMENTS

- IC-F14/F15 -

CHANNEL	FREQUENCY	SETTING CONDITION	CHANNEL	FREQUENCY	SETTING CONDITION
1	174.000 MHz	Set TX power to High.	6	155.000 MHz	Set TX power to Low1. Set IF bandwidth to Narrow.
2	174.000 MHz	Set TX power to Low2.	7	155.000 MHz	Set TX power to Low1. Set IF bandwidth to Wide/Middle. (Middle : EUR only)
3	174.000 MHz	Set TX power to Low1.			
4	174.000 MHz	Set TX power to Low1. Set DTCS code to 007. Set IF bandwidth to Narrow.	8	155.000MHz	Set TX power to Low1. Set IF bandwidth to Wide. Set CTCSS to 151.400Hz.
5	174.000 MHz	Set TX power to Low1. Set DTCS code to 007. Set IF bandwidth to Wide/Middle. (Middle : EUR only)	9	136.000 MHz	Set IF bandwidth to Wide.

- IC-F14S/F15S -

- Clone adjustment frequency and setting condition everytime adjusting each item (1-8).

1.PLL LOCK VOLTAGE

CH.	FREQUENCY	SETTING CONDITION
1	174.000 MHz	Set TX power to Low1.
2	136.000 MHz	Set IF bandwidth to Wide.

2.REFERENCE FREQUENCY

CH.	FREQUENCY	SETTING CONDITION
1	174.000 MHz	Set TX power to Low1.

3.TX POWER

CH.	FREQUENCY	SETTING CONDITION
1	174.000 MHz	Set TX power to High.
2	174.000 MHz	Set TX power to Low2.
3	174.000 MHz	Set TX power to Low1.

4.FM DEVIATION

CH.	FREQUENCY	SETTING CONDITION
1	155.000 MHz	Set TX power to Low1. Set IF bandwidth to Narrow.
2	155.000 MHz	Set TX power to Low1. Set IF bandwidth to Wide/Middle. (Middle : EUR only)

5.MODULATION BALANCE

CH.	FREQUENCY	SETTING CONDITION
1	174.000 MHz	Set TX power to Low1. Set DTCS code to 007. Set IF bandwidth to Narrow.
2	174.000 MHz	Set TX power to Low1. Set DTCS code to 007. Set IF bandwidth to Wide/Middle. (Middle : EUR only)

6.CTCSS/DTCS DEVIATION

CH.	FREQUENCY	SETTING CONDITION
1	155.000MHz	Set TX power to Low1. Set IF bandwidth to Wide. Set CTCSS to 151.400Hz.

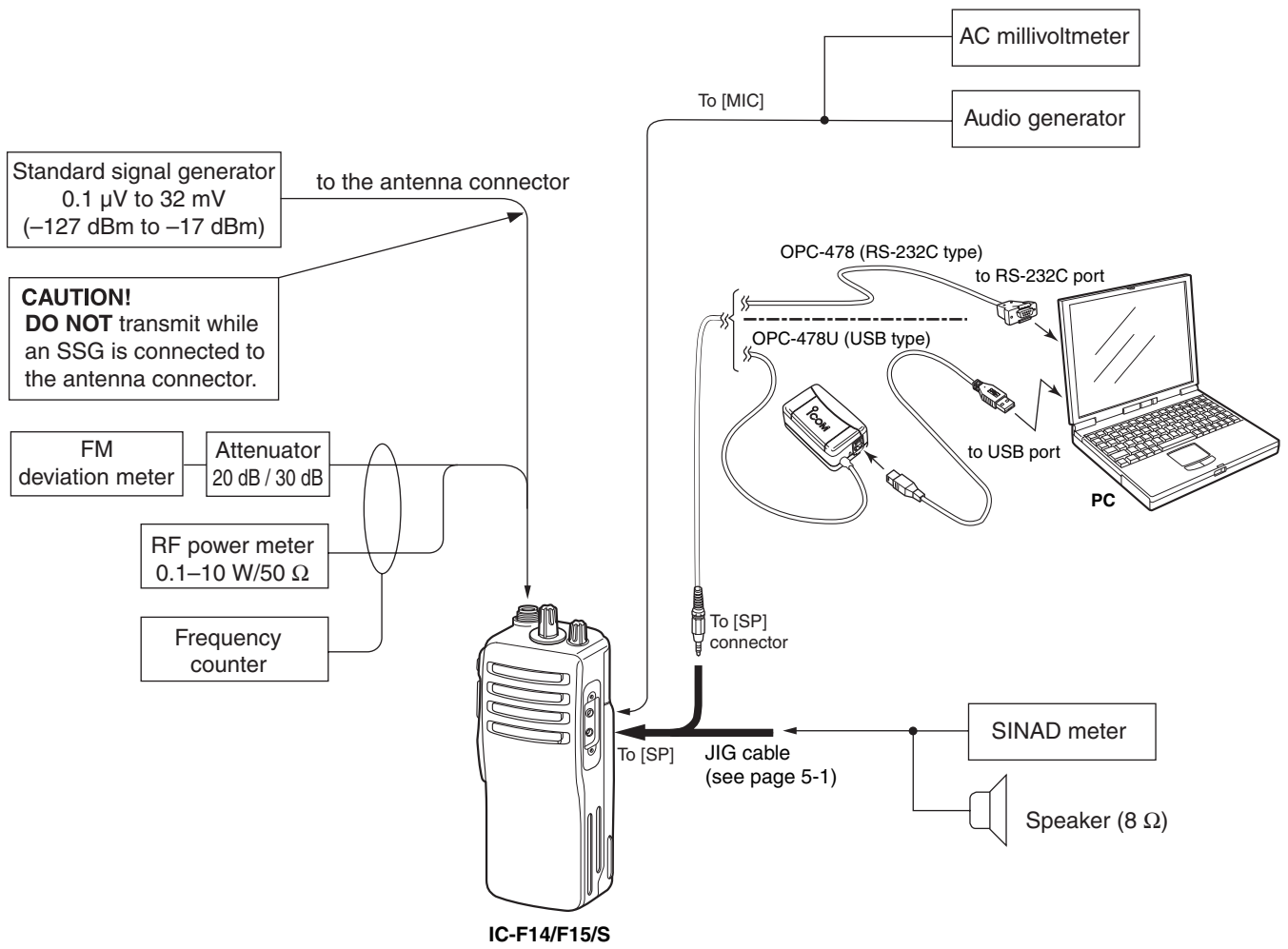
7.RX SENSITIVITY

CH.	FREQUENCY	SETTING CONDITION
1	136.000 MHz	Set IF bandwidth to Wide.

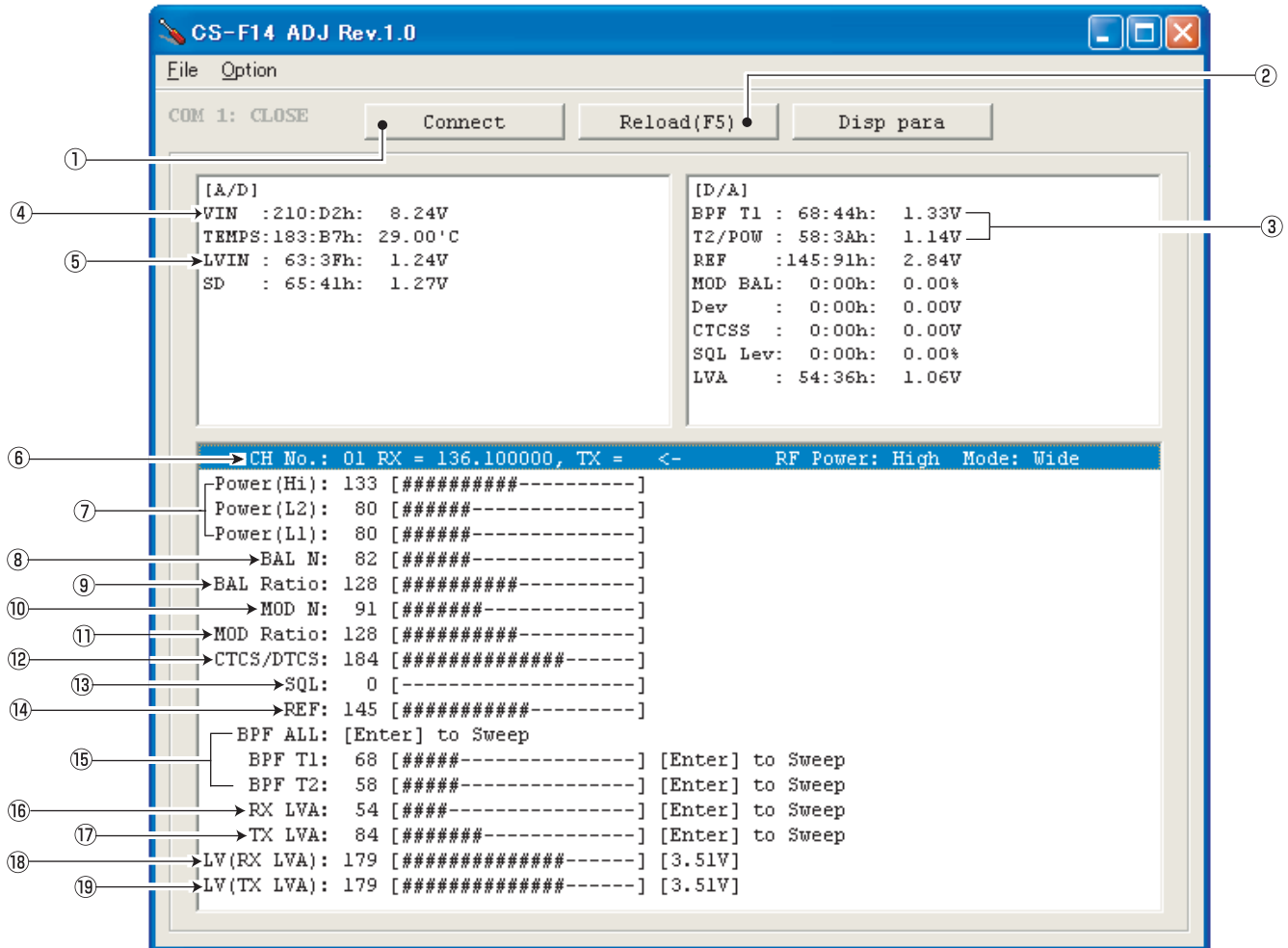
8.SQUELCH LEVEL

CH.	FREQUENCY	SETTING CONDITION
1	155.000MHz	Set TX power to Low1. Set IF bandwidth to Wide.

• CONNECTION



• PC SCREEN EXAMPLE



NOTE: The above screen is an example.
Each transceiver has its own specific values for each setting.

- | | |
|-------------------------------------|--|
| ①: Transceiver's connection state | ⑫: CTCSS/DTCS deviation |
| ②: Reload adjustment data | ⑬: Squelch level |
| ③: Receive sensitivity measurement | ⑭: Reference frequency |
| ④: Connected DC voltage measurement | ⑮: Receive sensitivity (automatically) |
| ⑤: PLL lock voltage measurement | ⑯: PLL lock voltage for RX (automatically) |
| ⑥: Operating channel select | ⑰: PLL lock voltage for TX (automatically) |
| ⑦: RF output power | ⑱: PLL lock voltage for RX (manually) |
| ⑧: FM deviation balance (Narrow) | |
| ⑨: FM deviation balance (Wide) | |
| ⑩: FM deviation (Narrow) | |
| ⑪: FM deviation (Wide) | |

5-3 SOFTWARE ADJUSTMENTS (TRANSMITTING)

Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard.

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE
		UNIT	LOCATION	
PLL LOCK VOLTAGE [LV (RX LVA)] [LV (TX LVA)]	1 • Operating CH : CH3 (*CH1) • Receiving	PC screen	Check the "LV" item on the CS-F14 ADJ's screen.	3.5 V
	2 • Operating CH : CH3 (*CH1) • Connect an RF power meter or 50 Ω dummy load to the antenna connector. • Transmitting			3.5 V
	3 • Operating CH : CH9 (*CH2) • Receiving	MAIN	Connect the digital multimeter to the "LV" line.	0.9–1.5 V (Verify)
	4 • Operating CH : CH9 (*CH2) • Transmitting			0.9–1.5 V (Verify)
REFERENCE FREQUENCY [REF]	1 • Operating CH : CH3 (*CH1) • Transmitting	Top panel	Loosely couple the frequency counter to the antenna connector.	174.0000 MHz
OUTPUT POWER [Power (Hi)] [Power (L2)] [Power (L1)]	1 • Operating CH : CH1 (*CH1) • Transmitting	Top panel	Connect the RF power meter to the antenna connector.	5.0 W
	2 • Operating CH : CH2 (*CH2) • Transmitting			2.0 W
	3 • Operating CH : CH3 (*CH3) • Transmitting			1.0 W
FM DEVIATION [MOD N] (Narrow) [MOD Ratio] (Middle; EUR only) [MOD Ratio] (Wide)	1 • Operating CH : CH6 (*CH1) • Set the deviation meter as: HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P_P)/2 • Connect the audio generator the [MIC] connector and set as : 1.0 kHz • Transmitting	Top panel	Connect the FM deviation meter to the antenna connector through the attenuator.	±2.10 kHz
	2 • Operating CH : CH7 (*CH2) • Transmitting			±3.20 kHz
	3 • Operating CH : CH7 (*CH2) • Transmitting			±4.10 kHz
MODULATION BALANCE [BAL N] (Narrow) [BAL Ratio] (Middle; EUR only) [BAL Ratio] (Wide)	1 • Operating CH : CH4 (*CH1) • No audio applied to the [MIC] input. • Set the deviation meter as: HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P_P)/2 • Transmitting	Top panel	Connect the FM deviation meter with the oscilloscope to the antenna connector through an attenuator.	<p>Set to square wave form</p> 
	2 • Operating CH : CH5 (*CH2) • Transmitting			
	3 • Operating CH : CH5 (*CH2) • Transmitting			
CTCSS/DTCS DEVIATION [CTCS/DTCS]	1 • Operating CH : CH8 (*CH1) • No audio applied to the [MIC] input. • Transmitting	Top panel	Connect the FM deviation meter to the antenna connector through the attenuator.	±0.68 kHz

*For F14S/F15S adjustment.

SOFTWARE ADJUSTMENTS (RECEIVING)

- Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard.

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE	
		UNIT	LOCATION		
RX SENSITIVITY [BPF T1], [BPF T2]	1	<ul style="list-style-type: none"> • Operating CH : CH9 • Connect a standard signal generator to the antenna connector and set as: Frequency : 136.000 MHz Level : 10 μV (-87 dBm) Modulation : 1 kHz Deviation : \pm3.5 kHz • Receiving 	Side pannel	Connect a SINAD meter with an 8 Ω load to the [SP] jack through the JIG cable.	Minimum distortion level
	<p>CONVENIENT: The BPF T1, BPF T2 can be adjusted automatically. 1-1: Set the cursor to "BPF ALL" on the adjustment program and then push [ENTER] key. 1-2: The connected PC tunes BPF T1, BPF T2 to peak levels. or 2-1: Set the cursor to one of BPF T1, T2 as desired. 2-2: Push [ENTER] key to start tuning. 2-3: Repeat 2-1 and 2-2 to perform additional BPF tuning.</p>				
SQUELCH LEVEL [SQL]	1	<ul style="list-style-type: none"> • Operating CH : CH7 (*CH1) • Connect an SSG to the antenna connector and set as: Frequency : 155.000MHz Level : 0.18 μV (-122 dBm) Modulation : 1 kHz Deviation : \pm3.5 kHz • Receiving 	Side panel	Connect a speaker to the [SP] jack through the JIG cable	Set "SQL level" to close squelch. Then set "SQL level" at the point where the audio signals just appears.

*For F14S/F15S adjustment.

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
R183	7030006020	S.RES RR0510P-682-D (6.8 kΩ)	B	17.6/39.5
R184	7030008250	S.RES RR0510P-562-D (5.6 kΩ)	B	17.6/41.2
R185	7030005100	S.RES ERJ2GEJ 154 X (150 kΩ)	B	18.6/41.2
R186	7030005310	S.RES ERJ2GEJ 124 X (120 kΩ)	T	19.4/29.8
R187	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	B	9.1/18
R190	7030007280	S.RES ERJ2GEJ 331 X (330 Ω)	T	34.7/21.6
R191	7030008300	S.RES ERJ2GEJ 184 X (180 kΩ)	T	18/4.1
R192	7030005720	S.RES ERJ2GEJ 563 X (56 kΩ)	T	18/5.1
R193	7030005220	S.RES ERJ2GEJ 223 X (22 kΩ)	T	18/6.1
R194	7030005220	S.RES ERJ2GEJ 223 X (22 kΩ)	T	23.9/10.9
R195	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	T	19.7/4.1
R196	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	23.9/11.9
R197	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	23.9/12.9
R198	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	25.7/12.9
R200	7030005040	S.RES ERJ2GEJ 472 X (4.7 kΩ)	T	25.7/14.9
R201	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	23.9/14.9
R206	7030005110	S.RES ERJ2GEJ 224 X (220 kΩ)	T	13.4/4.1
R207	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	T	13.4/5.1
R208	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	15.6/5.1
R209	7030005220	S.RES ERJ2GEJ 223 X (22 kΩ)	T	15.6/6.1
R210	7030008010	S.RES ERJ2GEJ 123 X (12 kΩ)	T	15.6/4.1
R211	7030005070	S.RES ERJ2GEJ 683 X (68 kΩ)	T	27.1/4.1
R212	7030005070	S.RES ERJ2GEJ 683 X (68 kΩ)	T	27.1/5.1
R213	7030005070	S.RES ERJ2GEJ 683 X (68 kΩ)	T	27.1/6.1
R214	7030005070	S.RES ERJ2GEJ 683 X (68 kΩ)	T	29/7.1
R215	7030005070	S.RES ERJ2GEJ 683 X (68 kΩ)	T	30.8/6.1
R220	7030004980	S.RES ERJ2GEJ 101 X (100 Ω)	B	16.1/22.3
R221	7030004980	S.RES ERJ2GEJ 101 X (100 Ω)	B	66.5/13.7
R222	7030005060	S.RES ERJ2GEJ 333 X (33 kΩ) [Others]	B	64.4/8.7
	7030005220	S.RES ERJ2GEJ 223 X (22 kΩ) [EU1, EU2]	B	64.4/8.7
R223	7030005060	S.RES ERJ2GEJ 333 X (33 kΩ)	B	61.7/9.7
R224	7030005000	S.RES ERJ2GEJ 471 X (470 Ω)	B	75.5/10.3
R225	7030004980	S.RES ERJ2GEJ 101 X (100 Ω)	B	33.9/6.8
R226	7210003061	S.RES ERJ2GEJ 103 X (10 kΩ)	T	95/14
R227	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	T	95/14
R228	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	T	94.5/15.2
R229	7030005530	S.RES ERJ2GEJ 100 X (10 Ω)	T	86.4/10.1
R230	7030005530	S.RES ERJ2GEJ 100 X (10 Ω)	T	86.3/16.4
R231	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	T	90.6/2.8
R232	7030007300	S.RES ERJ2GEJ 332 X (3.3 kΩ)	T	93.2/4.3
R233	7030007300	S.RES ERJ2GEJ 332 X (3.3 kΩ)	T	92.6/2.8
R234	7030005100	S.RES ERJ2GEJ 154 X (150 kΩ)	B	23/6.4
R235	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	20.3/4.2
R236	7030005230	S.RES ERJ2GEJ 334 X (330 kΩ)	B	23/4.2
R237	7030009290	S.RES ERJ2GEJ 562 X (5.6 kΩ)	T	21.1/39.1
R238	7410001140	S.ARY EXB28V104JX	B	40.9/9.7
R240	7030005590	S.RES ERJ2GEJ 680 X (68 Ω)	T	100.3/12.3
R241	7030010040	S.RES ERJ2GE-JPW [US2, EU2, GE2]	T	39.4/7.1
R242	7030010040	S.RES ERJ2GE-JPW [US2, EU2, GE2]	T	41.4/7.1
R251	7030008010	S.RES ERJ2GEJ 123 X (12 kΩ)	B	5.9/9.1
R252	7030005530	S.RES ERJ2GEJ 100 X (10 Ω)	B	13.7/9.1
R254	7030008010	S.RES ERJ2GEJ 123 X (12 kΩ)	B	9.3/10.1
R255	7030008010	S.RES ERJ2GEJ 123 X (12 kΩ)	B	7.6/10.1
R256	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	T	6/8.5
R257	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	T	9/22.1
R258	7410001140	S.ARY EXB28V104JX	T	6.6/20.6
R259	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	T	21.6/22.1
R260	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	T	20.1/24.7
R261	7410001130	S.ARY EXB28V102JX	T	19.4/19.9
R262	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	T	21.3/13.9
R263	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	T	21.3/12.9
R264	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	21.3/10.9
R265	7410001130	S.ARY EXB28V102JX	T	19.7/9.2
R266	7030007340	S.RES ERJ2GEJ 153 X (15 kΩ)	T	5.7/18.8
R271	7030005160	S.RES ERJ2GEJ 105 X (1 MΩ)	B	9.5/39.5
R272	7030005160	S.RES ERJ2GEJ 105 X (1 MΩ)	B	10.5/39.5
R273	7030005160	S.RES ERJ2GEJ 105 X (1 MΩ)	B	11.5/39.5
R274	7030005070	S.RES ERJ2GEJ 683 X (68 kΩ)	B	14.5/39.5
R275	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	12.5/39.5
R276	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	7.5/39.5
R277	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	8.5/39.5
R278	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	13.5/39.5
R280	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	B	16.4/35.8
R284	7030004980	S.RES ERJ2GEJ 101 X (100 Ω)	B	16/26.2

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
R287	7030007280	S.RES ERJ2GEJ 331 X (330 Ω)	T	18.5/24.7
R288	7030005030	S.RES ERJ2GEJ 152 X (1.5 kΩ)	T	14.7/23.1
R291	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	5.9/12.5
R292	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	7.6/12.5
R293	7030008290	S.RES ERJ2GEJ 183 X (18 kΩ)	T	61.4/43.4
R294	7030005600	S.RES ERJ2GEJ 273 X (27 kΩ)	T	60.4/43.4
R295	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	B	95.1/43.4
R301	7030004980	S.RES ERJ2GEJ 101 X (100 Ω)	B	37.1/41.2
R302	7030004980	S.RES ERJ2GEJ 101 X (100 Ω)	B	37.1/43.1
R303	7030009290	S.RES ERJ2GEJ 562 X (5.6 kΩ)	B	36.1/41.2
R304	7030009290	S.RES ERJ2GEJ 562 X (5.6 kΩ)	B	36.1/43.1
R305	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	B	36.1/39.5
R306	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	B	35.1/41.2
R307	7030003350	S.RES ERJ3GEJY 181 V (180 Ω)	T	94.4/34.9
C2	4030017620	S.CER ECJ0EC1H100C	B	94.5/38.5
C3	4030017410	S.CER ECJ0EC1H240J	B	96.5/36.2
C4	4030017380	S.CER ECJ0EC1H050B	B	92.7/36.2
C5	4030017650	S.CER ECJ0EC1H270J	B	96.3/33.9
C6	4030017460	S.CER ECJ0EB1E102K	B	92.8/33.9
C7	4030017460	S.CER ECJ0EB1E102K	B	93.5/29.5
C8	4030017390	S.CER ECJ0EC1H180J	B	93.3/28.2
C9	4030017640	S.CER ECJ0EC1H150J	B	93.3/23.2
C10	4030017460	S.CER ECJ0EB1E102K	B	93.3/22.1
C11	4030009990	S.CER C1608 CH 1H 200J-T	B	91.7/21.9
C12	4030007090	S.CER C1608 CH 1H 470J-T	B	89.8/21.7
C13	4030010000	S.CER C1608 CH 1H 510J-T	B	87.9/20.9
C14	4030011530	S.CER C1608 CH 1H 110J-T	B	90.7/33.4
C15	4030017460	S.CER ECJ0EB1E102K	B	93.6/16
C16	4030017400	S.CER ECJ0EC1H220J	B	89.6/34.6
C17	4030017630	S.CER ECJ0EC1H120J	B	85.1/36.7
C18	4030017380	S.CER ECJ0EC1H050B	B	85.1/37.7
C19	4030017460	S.CER ECJ0EB1E102K	B	85.1/33.4
C20	4030017430	S.CER ECJ0EC1H101J	B	81.7/37.2
C22	4030017550	S.CER ECJ0EC1H1R5B	B	81.7/37.7
C23	4030018860	S.CER ECJ0EB0J105K	T	74.7/37.2
C24	4030017460	S.CER ECJ0EB1E102K	T	82.3/35.7
C25	4030017580	S.CER ECJ0EC1H060C	B	83.4/37.7
C26	4030017430	S.CER ECJ0EC1H101J	B	78.2/33.4
C27	4030017460	S.CER ECJ0EB1E102K	T	78.8/35.7
C28	4030017370	S.CER ECJ0EC1H3R5B	B	80/36.7
C29	4030017370	S.CER ECJ0EC1H3R5B	B	80/37.7
C30	4030016930	S.CER ECJ0EB1A104K	T	77.1/39.7
C31	4030016930	S.CER ECJ0EB1A104K	T	78.8/38.9
C32	4030017460	S.CER ECJ0EB1E102K	B	76.8/39.9
C33	4030017420	S.CER ECJ0EC1H470J	B	75.8/39.9
C36	4030017460	S.CER ECJ0EB1E102K	B	74.8/35.6
C37	4030016790	S.CER ECJ0EB1C103K	B	75.8/37.7
C38	4030017360	S.CER ECJ0EC1H030B	B	74.8/37.7
C39	4030017460	S.CER ECJ0EB1E102K	B	73.7/35.6
C40	4030017550	S.CER ECJ0EC1H1R5B	B	72.9/39.4
C41	4030017620	S.CER ECJ0EC1H100C	B	68.5/39.2
C42	4030017460	S.CER ECJ0EB1E102K	T	68.9/38.5
C43	4030017460	S.CER ECJ0EB1E102K	T	68.9/39.5
C44	4030017570	S.CER ECJ0EC1H040B	B	69/37.8
C45	4030017460	S.CER ECJ0EB1E102K	B	72.2/35.6
C48	4030016790	S.CER ECJ0EB1C103K	B	64.2/37.2
C49	4030017350	S.CER ECJ0EC1H020B	B	64.2/40
C50	4030017460	S.CER ECJ0EB1E102K	B	64.2/36.1
C51	4030017460	S.CER ECJ0EB1E102K	B	66.1/32.1
C52	4030017620	S.CER ECJ0EC1H100C	B	66.1/35.7
C53	4030016790	S.CER ECJ0EB1C103K	B	64.2/33.1
C54	4030017460	S.CER ECJ0EB1E102K	B	64.2/32.1
C55	4030017570	S.CER ECJ0EC1H040B	B	64.2/31.1
C56	4030017400	S.CER ECJ0EC1H220J	B	64.3/24.4
C57	4030017460	S.CER ECJ0EB1E102K	T	64.1/36.6
C58	4030017460	S.CER ECJ0EB1E102K	B	53.9/24.3
C59	4030017460	S.CER ECJ0EB1E102K	B	49.5/25.2
C60	4030016790	S.CER ECJ0EB1C103K	B	52.5/26.9
C61	4030017430	S.CER ECJ0EC1H101J	B	49.5/22.7
C62	4030017680	S.CER ECJ0EC1H820J	B	47.5/17.6
C63	4030017420	S.CER ECJ0EC1H470J	B	46.5/20.4
C64	4030016790	S.CER ECJ0EB1C103K	T	49.6/16.3

M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)

US1=F14 for USA, EU1=F14 for EURO, GE1=F14 for GEN S.=Surface mount

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
C258	4030017790	S.CER ECJ0EB1E682K	T	30.6/39.1
C259	4030018860	S.CER ECJ0EB0J105K	T	26.9/41.1
C260	4030017730	S.CER ECJ0EB1E471K	T	28.6/39.1
C261	4030016930	S.CER ECJ0EB1A104K	T	26.9/40.1
C264	4510004630	S.ELE ECEV1CA100SR	B	69.7/15.5
C265	4030017460	S.CER ECJ0EB1E102K	B	65/12.9
C266	4030016930	S.CER ECJ0EB1A104K	B	63.4/8.7
C269	4030017720	S.CER ECJ0EB1H331K	T	11.6/37.8
C270	4030016950	S.CER ECJ0EB1A473K	T	14.3/28.8
C271	4030016950	S.CER ECJ0EB1A473K	T	14.3/27.8
C272	4030016950	S.CER ECJ0EB1A473K	T	9.5/28.8
C273	4030016950	S.CER ECJ0EB1A473K	T	12.6/28.8
C274	4030016950	S.CER ECJ0EB1A473K	T	10/32.6
C275	4030016970	S.CER ECJ0EB1C223K	T	11.6/34.4
C276	4030016950	S.CER ECJ0EB1A473K	T	12.6/34.4
C277	4030016930	S.CER ECJ0EB1A104K	T	12.6/37.8
C278	4030017430	S.CER ECJ0EC1H101J	T	16.4/39.9
C279	4030018910	S.CER C1608 JB OJ 475K-T	T	36.8/21.6
C280	4030018110	S.CER ECJ0EB1H272K	T	21.1/27.8
C281	4030017780	S.CER ECJ0EB1E472K	T	17.7/26.8
C282	4030017710	S.CER ECJ0EC1H181J	T	17.7/29.8
C283	4030018900	S.CER ECJ0EB0J474K	T	19.4/31.7
C284	4030016930	S.CER ECJ0EB1A104K	T	22.9/39.1
C285	4030016930	S.CER ECJ0EB1A104K	T	22.9/40.1
C286	4030017460	S.CER ECJ0EB1E102K	B	16.6/41.2
C287	4550006250	S.TAN TEESVA 1A 106M8L	B	22.1/40.7
C288	4030017460	S.CER ECJ0EB1E102K	B	18.6/39.5
C289	4030016930	S.CER ECJ0EB1A104K	B	19.5/30.2
C290	4030017920	S.CER ECJ0EB1A683K	T	27.5/16.1
C291	4030016780	S.CER ECJ0EB1C153K	T	25.7/10.9
C292	4030016930	S.CER ECJ0EB1A104K	T	25.7/13.9
C293	4030017740	S.CER ECJ0EB1E821K	T	25.7/11.9
C294	4030016930	S.CER ECJ0EB1A104K	T	23.9/13.9
C295	4030018110	S.CER ECJ0EB1H272K	T	29/5.1
C296	4030018240	S.CER ECJ0EB1E562K	T	29/6.1
C297	4030017710	S.CER ECJ0EC1H181J	T	27.1/7.1
C298	4030018090	S.CER ECJ0EB1C822K	T	30.8/7.1
C299	4030017510	S.CER ECJ0EC1H680J	T	30.8/5.1
C300	4030017450	S.CER ECJ0EB1E271K	T	18.4/39.9
C306	4030017460	S.CER ECJ0EB1E102K	B	61.7/10.7
C307	4030017460	S.CER ECJ0EB1E102K	B	61.7/8.2
C308	4030017460	S.CER ECJ0EB1E102K	T	75.7/9.8
C309	4030017460	S.CER ECJ0EB1E102K	B	75.5/11.3
C310	4030016930	S.CER ECJ0EB1A104K	T	21.3/11.9
C311	4030017460	S.CER ECJ0EB1E102K	B	65.4/8.7
C312	4030017420	S.CER ECJ0EC1H470J	B	74.5/6.1
C313	4030017420	S.CER ECJ0EC1H470J	B	33.9/7.8
C314	4030017460	S.CER ECJ0EB1E102K	T	86.6/3.3
C315	4030017460	S.CER ECJ0EB1E102K	T	93.2/5.9
C316	4030016930	S.CER ECJ0EB1A104K	T	91.6/2.8
C317	4550007080	S.TAN TEESVA 1C 106M8R	B	93/11.3
C318	4030016930	S.CER ECJ0EB1A104K	T	90.4/10.1
C319	4030016930	S.CER ECJ0EB1A104K	T	89.6/3.7
C320	4030017730	S.CER ECJ0EB1E471K	T	88.6/3.7
C321	4030017460	S.CER ECJ0EB1E102K	B	19.3/4.2
C322	4030016950	S.CER ECJ0EB1A473K	T	94/14
C323	4030016950	S.CER ECJ0EB1A473K	T	88.1/10.1
C324	4030017420	S.CER ECJ0EC1H470J	T	85.2/14.1
C325	4550006250	S.TAN TEESVA 1A 106M8L	T	89.4/17.6
C326	4510006940	S.ELE EEVFC0J101P	B	87.8/8.9
C335	4030018860	S.CER ECJ0EB0J105K	B	57.2/21.1
C339	4030016930	S.CER ECJ0EB1A104K	B	5.9/17.2
C340	4030016930	S.CER ECJ0EB1A104K	B	9.3/12.5
C341	4030016930	S.CER ECJ0EB1A104K	B	5.9/10.1
C342	4030017630	S.CER ECJ0EC1H120J	B	18.3/4.2
C343	4030017580	S.CER ECJ0EC1H060C	B	5.6/4.2
C344	4030017640	S.CER ECJ0EC1H150J	B	7.6/9.1
C345	4030016930	S.CER ECJ0EB1A104K	B	11/11.2
C346	4030016930	S.CER ECJ0EB1A104K	B	11/10.1
C347	4030016790	S.CER ECJ0EB1C103K	T	8.9/6.3
C348	4030016930	S.CER ECJ0EB1A104K	T	6/10
C349	4030016930	S.CER ECJ0EB1A104K	T	21.3/14.9
C350	4030017460	S.CER ECJ0EB1E102K	T	59.4/43.4

M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
J1	6510021900	S.CNR BM02B-ASRS-TF	T	86.6/6.8
J2	6450001680	CNR HSJ1122-010010		
J3	6450002250	CNR HSJ1456-010320		
J4	6510018430	S.CNR AXN330C038P	B	11.8/30.6
J5	6510021900	S.CNR BM02B-ASRS-TF [US2, EU2, GE2]	T	50.4/11.7
F1	5210000830	S.FUS ERBFE3R00U	T	98/14.8
DS1	5040002670	S.LED CL-165HR/YG	T	102.8/12.4
MC1	7700002540	MIC SKP-4538		
S1	2260002840	SW SKHLLFA010		
S2	2260002800	S.SW SW-167 (SKQTLAE010)	B	99.4/44.2
S3	2260002800	S.SW SW-167 (SKQTLAE010)	B	60.9/44.2
S4	2250000490	ECR TP70TF5163-15.9F-2775 [US1, EU1, GE1]		
EP1	0910057892	PCB		
EP2	6910015600	S.BEA ACZ1005Y-241 (240 Ω)	T	77.4/22.2
EP3	6910015370	S.BEA ACZ1005Y-102-T	T	34.7/32
EP4	6910015370	S.BEA ACZ1005Y-102-T	B	55.5/30.5
EP6	6910015370	S.BEA ACZ1005Y-102-T	T	44.3/35.9

[CHASSIS UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
J1	6910015910	CNR ANT CONNECTOR-104		
J2	6910015860	CNR IMSA-6277S-02A-G		
S1	2260002870	SW AS-243-A13 [US2, EU2, GE2]		
SP1	2510001060	SP K036NA500-47		
W1	8900009640	CBL OPC-963		
W2	8900009640	CBL OPC-963 [US2, EU2, GE2]		

[CONNECT UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
C501	4030017460	S.CER ECJ0EB1E102K		
C502	4030016930	S.CER ECJ0EB1A104K		
J501	6910016390	CNR IMSA-9230B-1-02Z145-PT1		
EP501	0910057910	PCB B-6160		

[ANT UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
EP601	0910057901	PCB B-6159B		

US1=F14 for USA, EU1=F14 for EURO, GE1=F14 for GEN S.=Surface mount

SECTION 7 MECHANICAL PARTS AND DISASSEMBLY

7-1 CABINET PARTS

[MAIN UNIT]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
J2	6450001680	HSJ1122-010010	1
J3	6450002250	HSJ1456-010320	1
R226	7210003060	TP76N00N-15F-10KA-2251	1
R315	7210003060	TP76N00N-15F-10KA-2251	1
S1	2260002840	SKHLLFA010	1
S4	2250000490	TP70TF5163-15.9F-2775	1
MC1	7700002540	SKP-4538	1

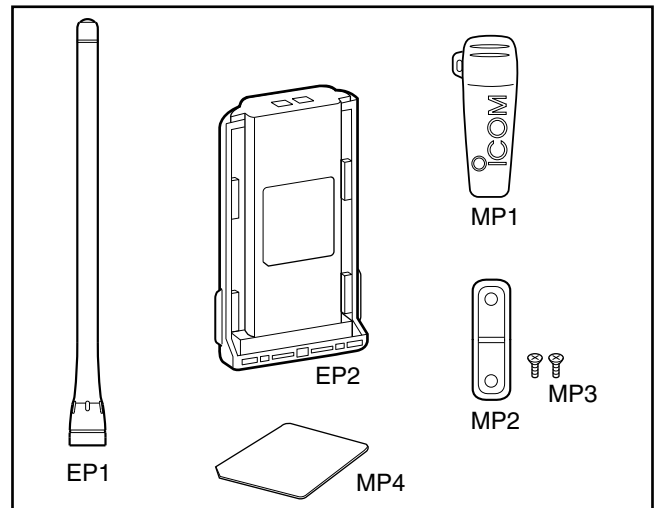
[CHASSIS PARTS]

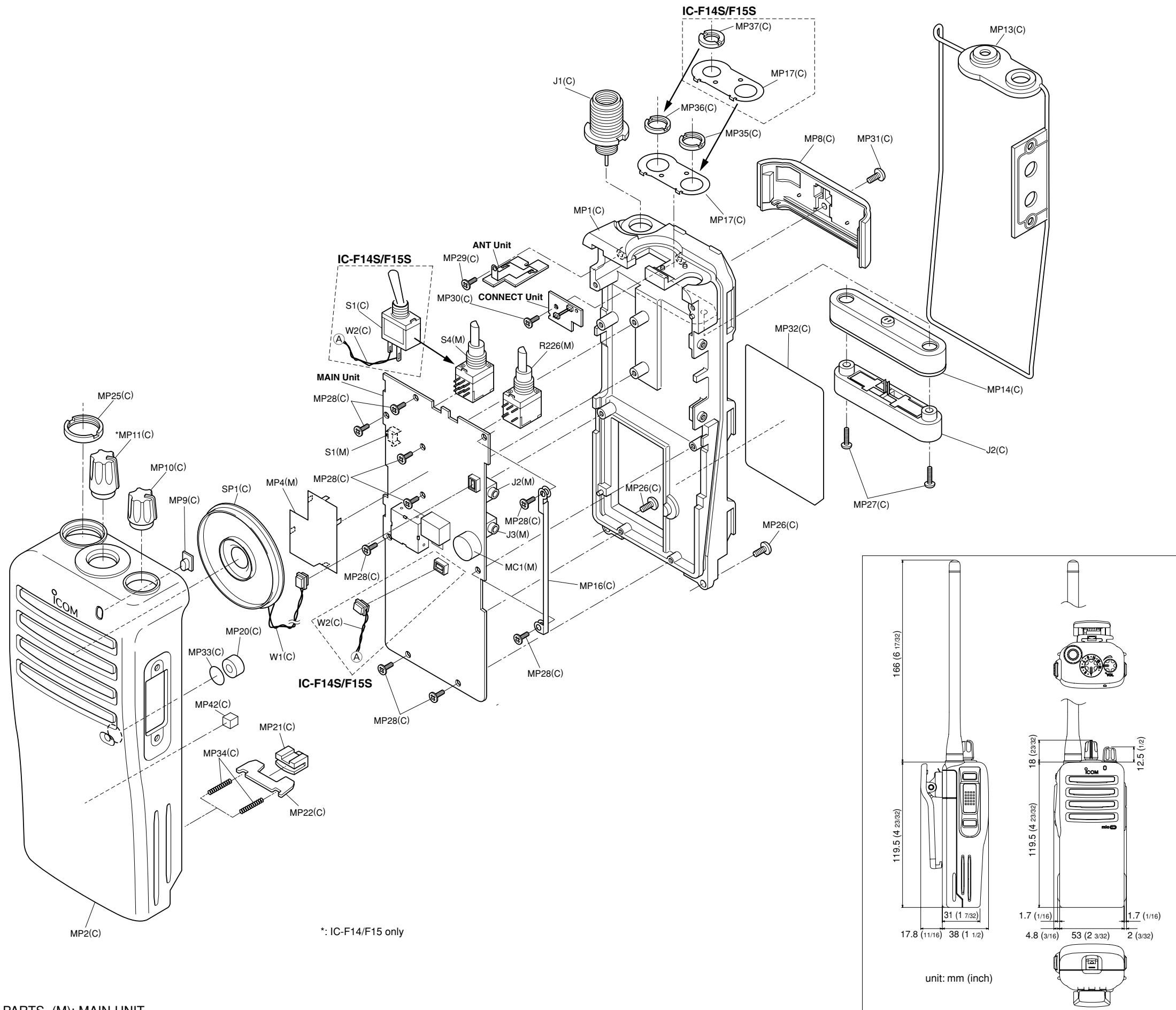
REF. NO.	ORDER NO.	DESCRIPTION	QTY.
S1	2260002870	AS-243-A13 [F14S], [F15S]	1
SP1	2510001060	K036NA500-47	1
W1	8900009640	OPC-963	1
W2	8900009640	OPC-963 [F14S], [F15S]	1
J1	6910015910	Antenna connector	1
J2	6910015860	IMSA-6277S-02A-G	1
MP1	8010019690	2775 chassis	1
MP2	8210020920	2775 front panel	1
	8210020910	2775 front panel (A) [F14S], [F15S]	1
MP4	8510016580	2775 shield plate	1
MP9	8930063350	2775 lens	1
MP10	8610011930	Knob N-318	1
MP11	8610012130	Knob N-323 [F14], [F15] only	1
MP13	8930063330	2775 B-main seal	1
	8930063340	2775 A-main seal [F14S], [F15S]	1
MP14	8930063060	2721 terminal rubber	1
MP16	8930063400	2775 side plate	1
MP17	8930063410	2775 B-top plate	1
	8930063420	2775 A-top plate [F14S], [F15S]	1
MP20	8930043760	1923 mic seal	1
MP21	8930059360	2600 release button	1
MP22	8930063390	2775 release plate	1
MP24	8610007920	Knob spring No.1500	1
MP25	8830001720	2721 antenna nut	1
MP26	8810009220	Screw B0 2 x 8 ZK (BT)	2
MP27	8810009560	Screw M2 x 6 ZK	2
MP28	8810009510	Screw M2 x 4 NI-ZU (BT)	9
MP29	8810009510	Screw M2 x 4 NI-ZU (BT)	1
MP30	8810009510	Screw M2 x 4 NI-ZU (BT)	1
MP31	8810010160	Screw M3 x 5 SUS ZK	1
MP32	8930051290	2251 opt sheet	1
MP33	8930042350	1922 mic sheet	1
MP35	8830001700	VR nut (Q)	1
MP36	8830001700	VR nut (Q)	1
MP37	8830001740	VR nut (S) [F14S], [F15S]	1
MP42	8930062230	Sponge (HN)	1

Screw abbreviations B0, BT: Self-tapping
 ZK: Black
 SUS: Stainless
 NI-ZU: Nickel-zinc

[ACCESSORIES]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
EP1	3310002321	FA-SC55V-1	1
EP2	0800007540	BP-231 ACC	1
MP1	8010019540	MB-94 ACC	1
MP2	8210020560	2721 JACK PANEL	1
MP3	8810004860	Screw M2 x 6 ZK	2
MP4	8930051290	2251 OPT SHEET	1



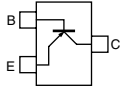
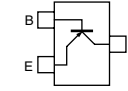
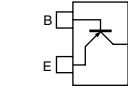
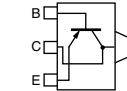
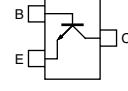
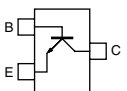
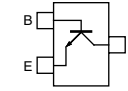
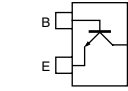
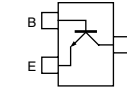
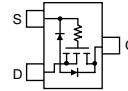
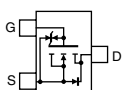
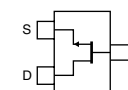
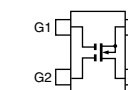
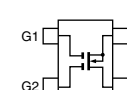
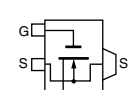
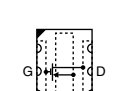
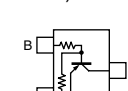
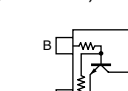
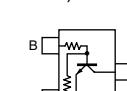
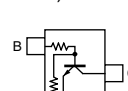
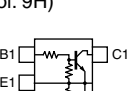
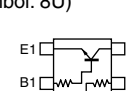
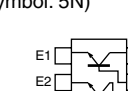


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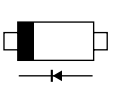
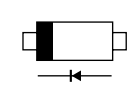
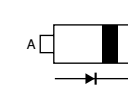
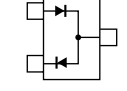
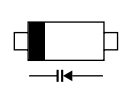
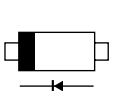
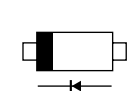
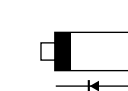
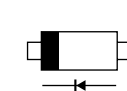
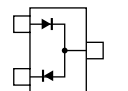
UNIT abbreviation (C): CHASSIS PARTS, (M): MAIN UNIT

SECTION 8 SEMI-CONDUCTOR INFORMATION

• TRANSISTOR AND FET's

2SA1576 R (Symbol: FR) 	2SA1577 Q (Symbol: HP) 	2SA2048TL R (Symbol: UL) 	2SB1132 R (Symbol: BARB) 	2SC4081 R (Symbol: BR) 
2SC4116 BL (Symbol: LL) 	2SC4226 R25 (Symbol: BR) 	2SC5107 (Symbol: MFO) 	2SC5110 (Symbol: MGO) 	2SK1829 (Symbol: K1) 
2SK3019 (Symbol: KN) 	2SK880 Y (Symbol: XY) 	3SK293 (Symbol: UF) 	3SK299 U73 (Symbol: U73) 	RD01MUS1 (Symbol: K2) 
RD07MVS1 (Symbol: RD07MVS1) 	UNR9113J (Symbol: 6C) 	UNR911HJ (Symbol: 6P) 	UNR9210J (Symbol: 8L) 	UNR9213J (Symbol: 8C) 
XP1214 (Symbol: 9H) 	XP4216 (Symbol: 8U) 	XP6501 AB (Symbol: 5N) 		

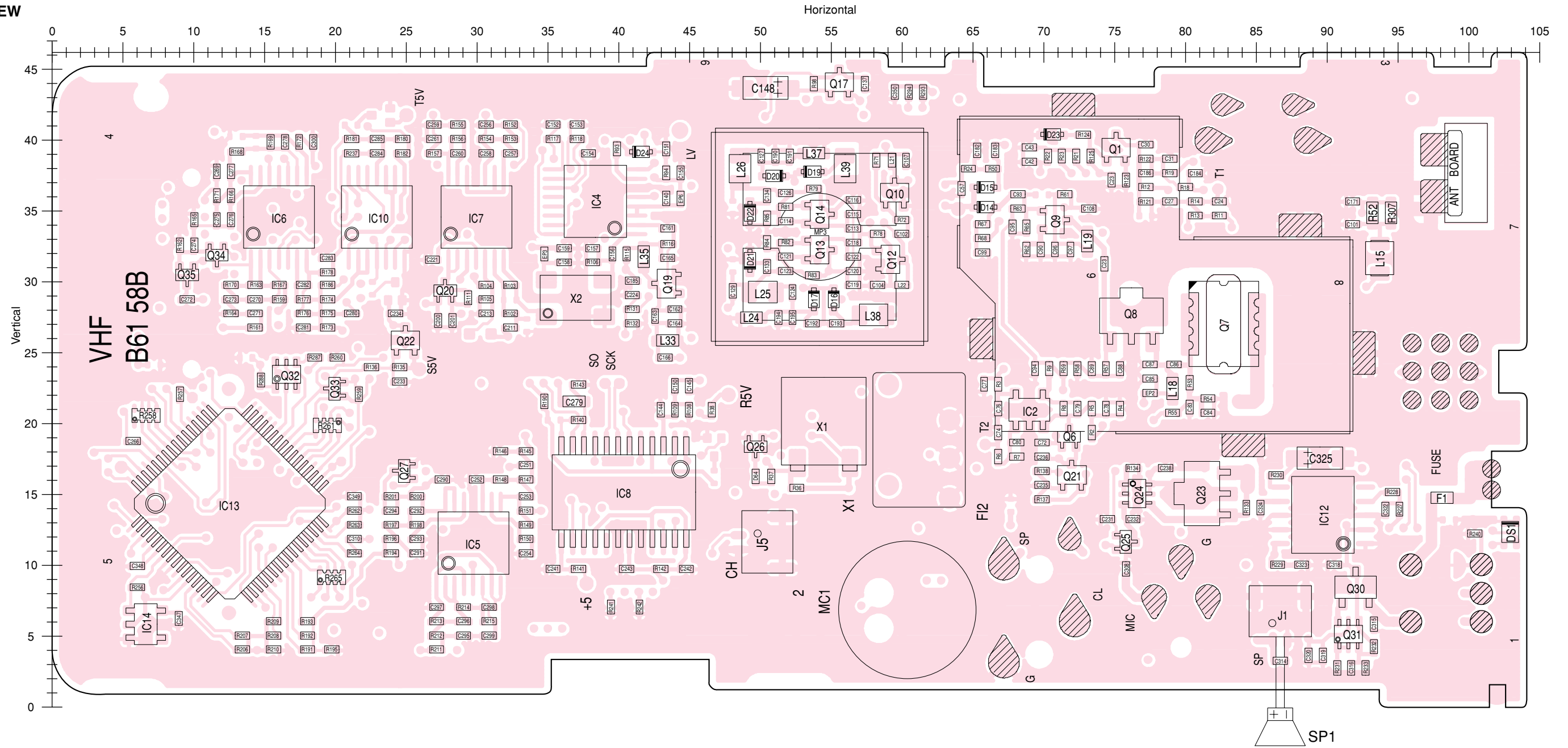
• DIODES

1SS400 (Symbol: A) 	1SV239 (Symbol: TC) 	1SV307 (Symbol: TX) 	DAN222 (Symbol: N) 	HVC350B (Symbol: B0) 
HVC375B (Symbol: B8) 	HVC376B (Symbol: B9) 	MA2S077 (Symbol: S) 	MA2S111 (Symbol: A) 	RB876W TL (Symbol: 3X) 

SECTION 9 BOARD LAYOUTS

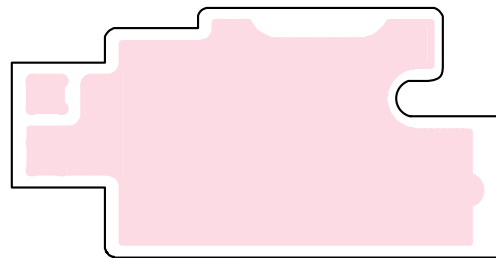
9-1 MAIN UNIT

• TOP VIEW



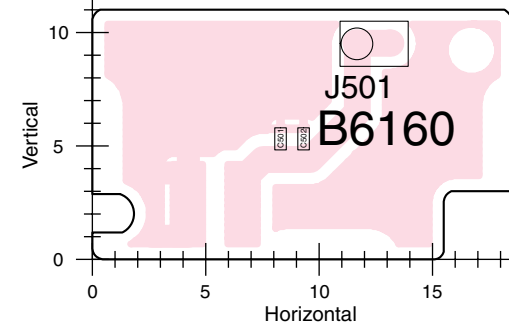
9-2 ANT UNIT

• TOP VIEW

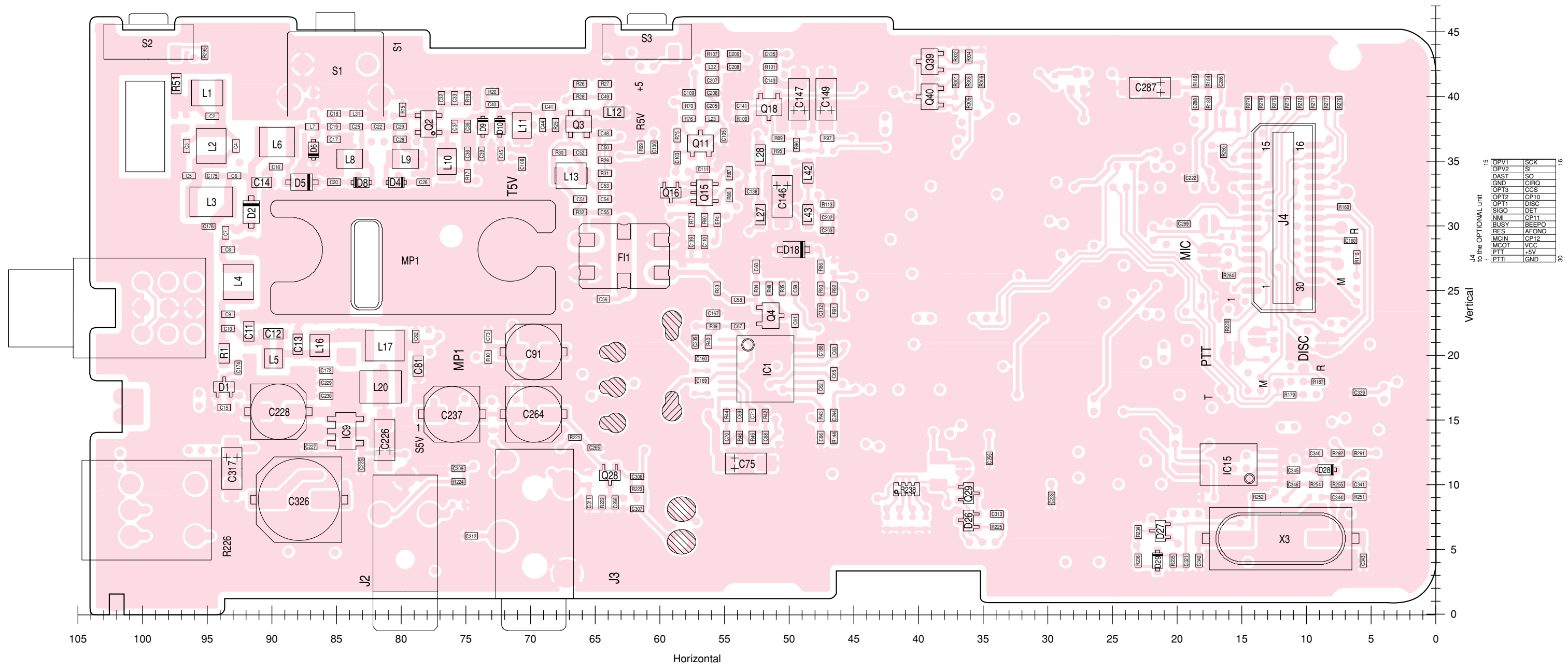


9-3 CONNECT UNIT

• TOP VIEW



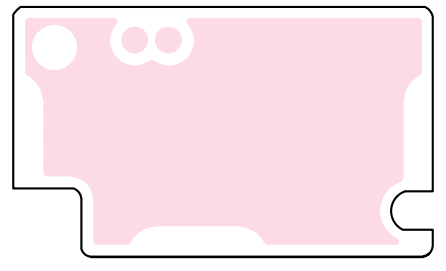
● BOTTOM VIEW



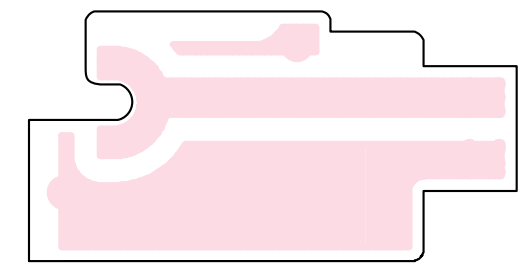
J4 to the OPTIONAL unit

15	OPV1	SCK
16	OPV2	SI
17	DAST	SO
18	GND	CIRG
19	OPT13	CSS
20	OPT2	CP10
21	OPT1	DISC
22	SIG0	DET
23	NMI	CP11
24	BUSY	BEEPO
25	RES	AFONO
26	MCIN	CP12
27	MCOT	VCC
28	PTT	L5V
29	PTT1	GND
30		

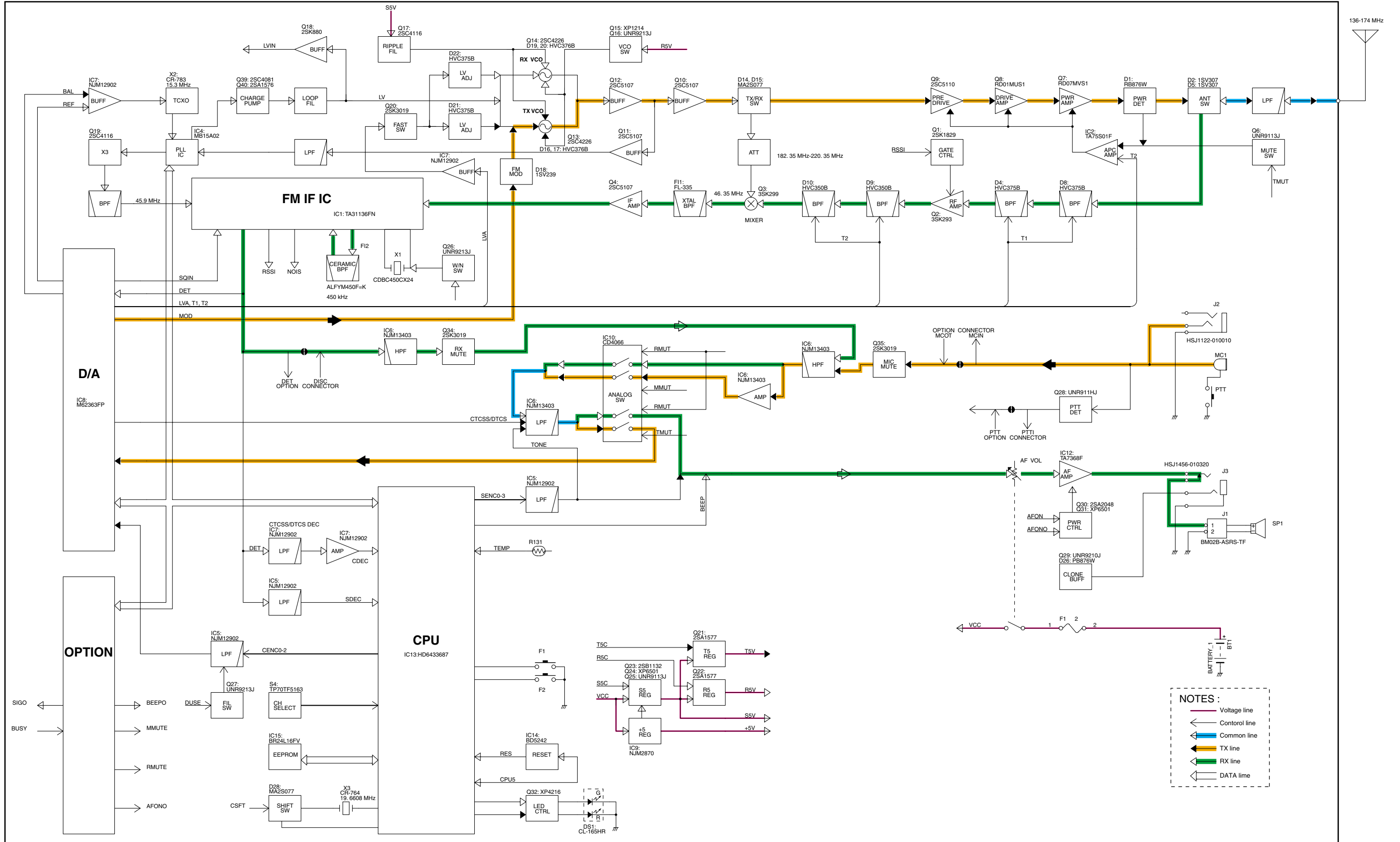
● BOTOM VIEW



● BOTOM VIEW



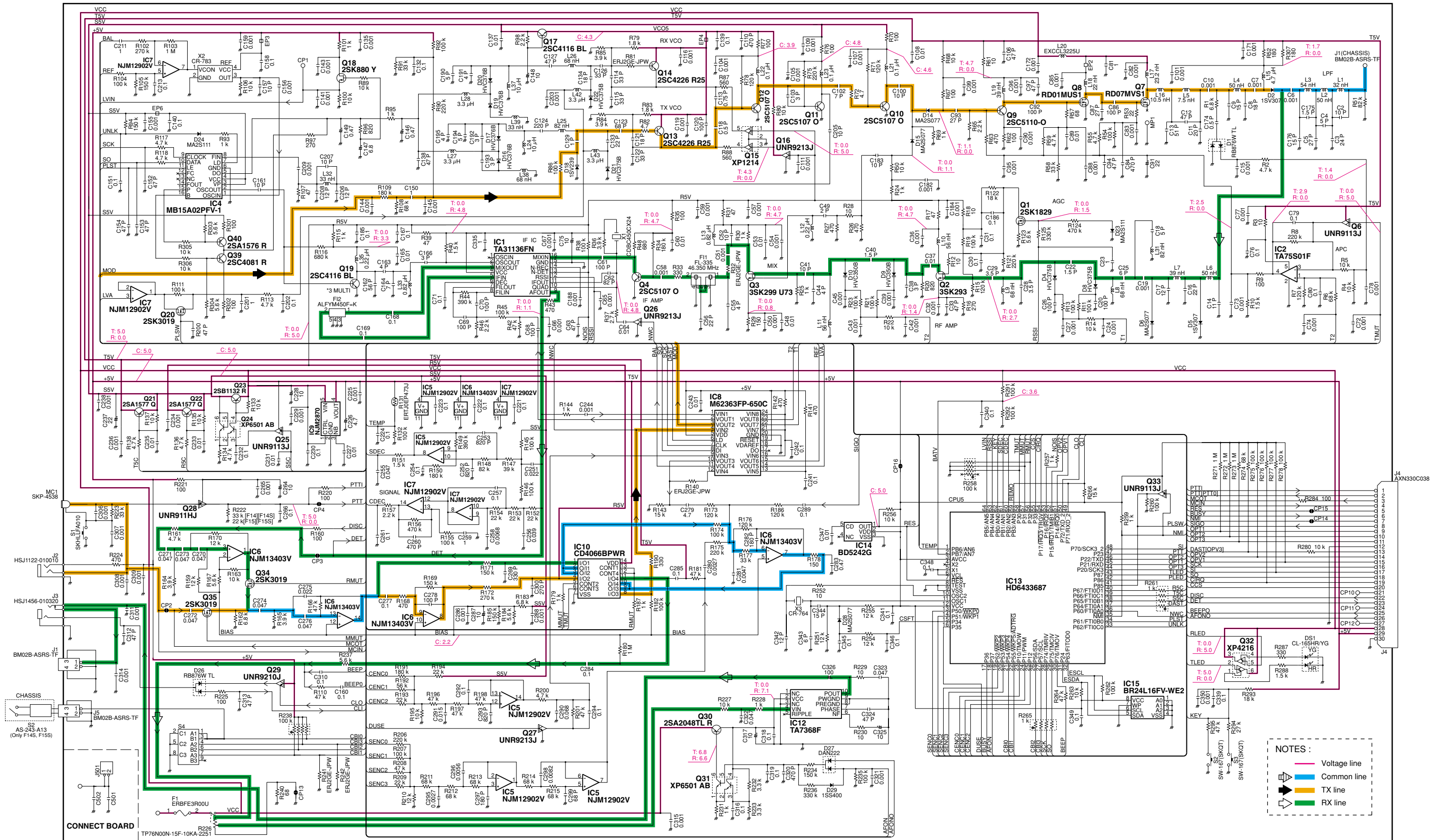
SECTION 10 BLOCK DIAGRAM



- NOTES:**
- Voltage line
 - Control line
 - Common line
 - TX line
 - RX line
 - DATA line

SECTION 11 VOLTAGE DIAGRAM

11-1 MAIN UNIT



NOTES:

- Voltage line
- Common line
- TX line
- RX line

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