

 **ICOM**

SERVICE MANUAL

VHF TRANSCEIVER

IC-F30GT
IC-F30GS
IC-F31GT
IC-F31GS

INTRODUCTION

This service manual describes the latest service information for the **IC-F30GT/GS** and **IC-F31GT/GS** VHF TRANSCEIVER at the time of publication.

To upgrade quality, all electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

DANGER

NEVER connect the transceiver to an AC outlet or to a DC power supply that uses more than 10 V. This will ruin the transceiver.

DO NOT expose the transceiver to rain, snow or any liquids.

DO NOT reverse the polarities of the power supply when connecting the transceiver.

DO NOT apply an RF signal of more than 20 dBm (100 mW) to the antenna connector. This could damage the transceiver's front end.

INTRINSICALLY SAFE QUALIFICATION

When servicing intrinsically safe versions of the **IC-F30GT/GS** and **IC-F31GT/GS** the following conditions must be met. Failing to satisfy any of these conditions will invalidate the INTRINSICALLY SAFE certification.

1. Servicing the transceiver should only be undertaken by suitably qualified personnel in a non-hazardous area. Never attempt to remove the case in a hazardous area.
2. **ONLY** the approved battery, ICOM's BP-210FM may be used.
3. **USE ONLY** safety critical components as specified in the parts list (SECTION 6), should replacement of any item be necessary.

ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

1110001810	S.IC TA7368F	IC-F30GT	MAIN UNIT	1 piece
8930053170	2337 Key board	IC-F31GS	CHASSIS	5 pieces

Addresses are provided on the inside back cover for your convenience.



REPAIR NOTES

1. Make sure a problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated tuning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 40 dB or 50 dB attenuator between the transceiver and a deviation meter or spectrum analyser when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.

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SECTION 1 SPECIFICATIONS

	USA/GEN	EUR
GENERAL	Measurement method	EIA-152-C/204D or TIA-603
	Frequency coverage	136.000–174.000 MHz
	Type of emission	16K0F3E [25 kHz; Wide], 8K50F3E [12.5 kHz; Narrow] 14K0F3E [20 kHz; Middle], 8K50F3E [12.5 kHz; Narrow]
	Number of conventional channels	Max. 256 ch (16 channels × 16 banks)
	Power supply requirement	7.2 V DC (negative ground; supplied battery pack)
	Current drain (approx.)	TX at High power 2.0 A RX rated audio 300 mA stand-by 95 mA (typical)
	Frequency error	±2.5 ppm
	Usable temperature range	−30°C to +60°C (−22°F to +140°F)
	Dimensions (proj. not included)	54(W) × 139(H) × 38(D) mm; 21½(W) × 51½(H) × 11½(D) inch
	Weight (approx.)	420 g; 14.8 oz (with BP-210)
TRANSMITTER	RF output power	5 W / 2 W / 1 W (High/Low2/Low1)
	Modulation system	Variable reactance frequency modulation
	Maximum permissible deviation	±5.0 kHz [Wide], ±2.5 kHz [Narrow]
	Spurious emissions	73 dBc typical
	Adjacent channel power	70 dB [Wide], 60 dB [Narrow]
	Audio frequency response	+2 dB to −8 dB of 6 dB/octave range from 300 Hz to 3000 Hz [Wide]/2550 Hz [Narrow]
	Audio harmonic distortion	3% typical at 1 kHz, 40% deviation
	FM hum and noise (typical)	46 dB [Wide], 40 dB [Narrow]
	Residual modulation (typical)	—
	Limiting charact of modulator	60–100% of max. deviation
RECEIVER	Ext. microphone connector	9-pin multi connector/2.2 kΩ
	Receive system	Double-conversion superheterodyne system
	Intermediate frequencies	1st: 31.65 MHz, 2nd: 450 kHz
	Sensitivity (typical)	0.25 µV at 12 dB SINAD
	Squelch sensitivity (at threshold) (typical)	0.25 µV
	Adjcent channel selectivity (typical)	73 dB [Wide], 63 dB [Narrow]
	Spurious response	70 dB
	Intermodulation (typical)	74 dB
	FM hum and noise (typical)	46 dB [Wide], 40 dB [Narrow]
	Hum and noise (with CCITT filter) (typical)	—

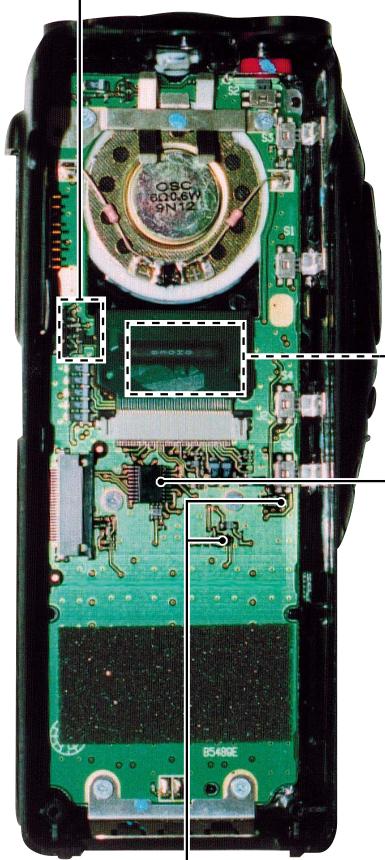
All stated specifications are subject to change without notice or obligation.

SECTION 2 INSIDE VIEWS

• FRONT UNIT

Bottom view

Internal speaker switch circuit
(Q6, Q7: CPH3403, Q8: 2SC4081,
Q9: DTC144EUA)



KEY LED switch
(Q1, Q2: 2SC4116)

• MAIN UNIT

Top view

Antenna switching
(D1, D25, D24: MA77
D1 is bottom side)

Power amplifier
(Q1: 2SK2974)

Pre-drive amplifier
(Q2: 2SK2973)

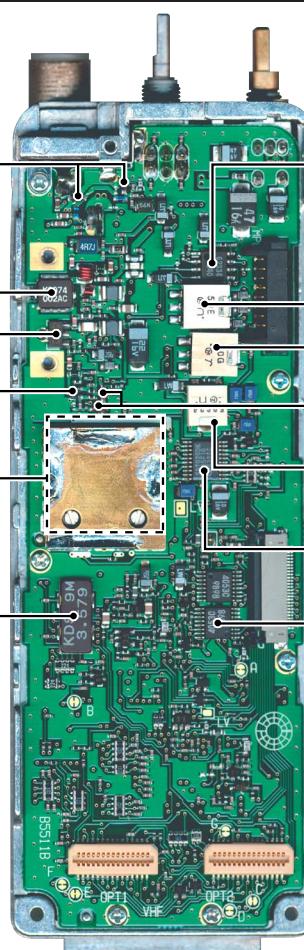
YGR amplifier
(Q3: 2SC4226)

TX/RX VCO circuit

3.58 MHz crystal
(X4: CR-563
3.579545 MHz)

LCD module
(DS10: EDMMU1FA0)

Expander IC
(IC1: TC74VHC373FT)



D/A converter
(IC27: M62334FP)

2nd IF filter (450 kHz)
(FI2: SFPCA450KE4A)
(FI3: SFPCA450KG1A)

TX/RX switch
(D5, D4: MA77)

Discreminator
(X2: CDBCB450KCA24 450 kHz)

PLL IC
(IC1: SA7025DK)

PTT/MD1 switch and
INT/EXT microphone switch
(IC19: BU4053BCF)

• MAIN UNIT

Bottom view

S5 regulator
(Q31: 2SA1362)

+5 regulator
(Q32: 2SB1132)

R5 regulator
(Q30: 2SA1362)

2nd mixer/IF detect
/SQL amplifier
(IC3: TA31136FN)

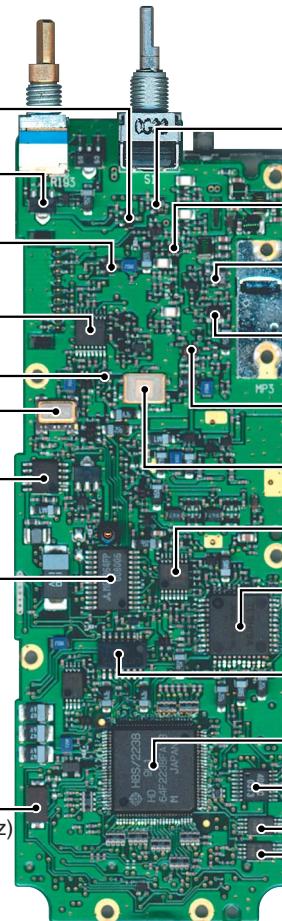
1st IF amplifier
(Q18: 2SC4215)

TCXO
(X1: CR-667
15.600 MHz)

AF amplifier
(IC5: TA7368F)

D/A converter
(IC13: M62364FP)

Crystal oscillator
for CPU clock
(X3: CR-681 12.288 MHz)



T5 regulator
(Q29: 2SA1362)

RF amplifier
(Q20: 3SK293)

Power detector
(D2: MA713)

APC amplifier
(IC4: TC75S51F)

1st mixer
(Q19: 3SK206)

1st IF filter
(FI1: FL-322 31.650 MHz)

Splatter filter
(IC7: NJM2902V)

Microphone amplifier/mute
/compander
(IC9: TC35453F)

DTMF decoder
(IC17: LC73872M)

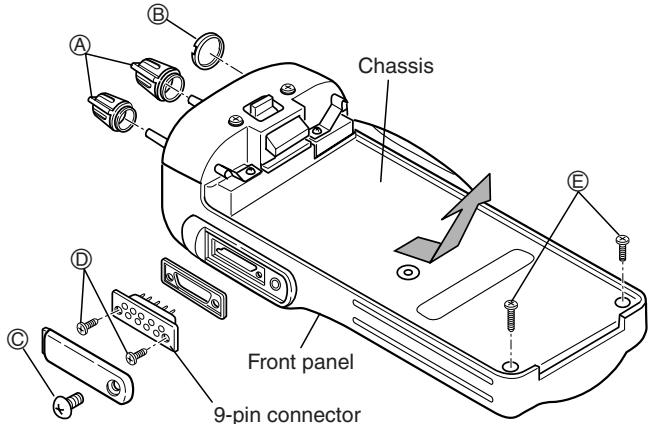
CPU
(IC14: HD64F2238FA13)

Expander IC
(IC23: BU4094BCFV)

EEPROM
(IC16, IC24: HN58X2464TI)

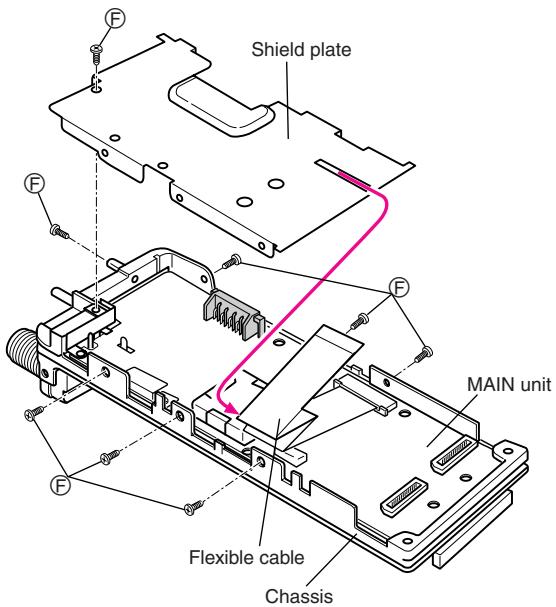
SECTION 3 DISASSEMBLY INSTRUCTIONS

1 Removing the chassis panel



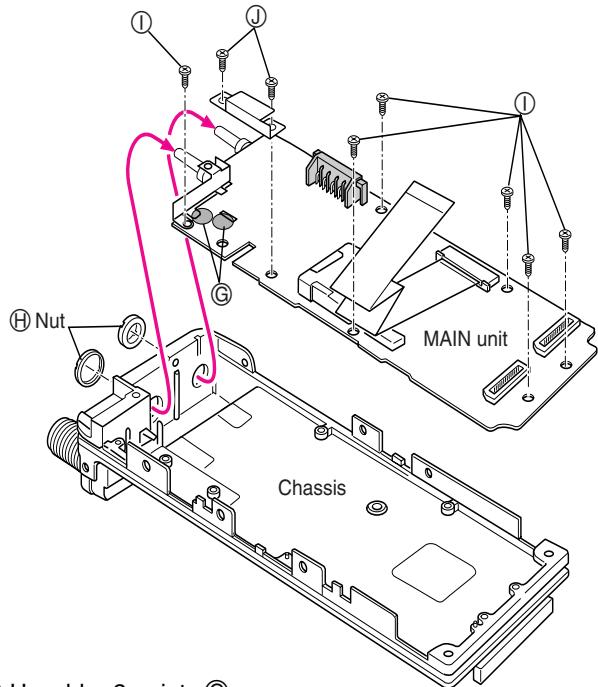
- ① Remove 2 knobs Ⓐ, and unscrew 1 nut Ⓑ.
- ② Unscrew 1 screw Ⓒ (ICOM screw), and 2 screws Ⓓ (2 × 4 mm, black) from the 9-pin connector.
- ③ Unscrew 2 screws Ⓔ (2 × 8 mm, silver) from the chassis.
- ④ Take off the chassis in the direction of the arrow.

2 Removing the shield plate



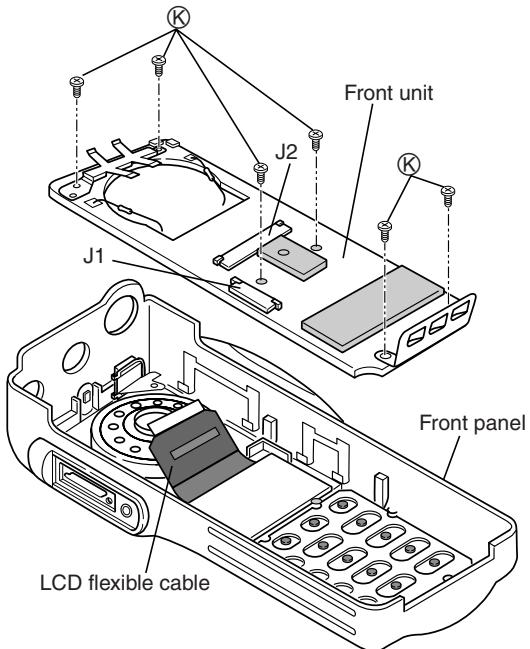
- ① Unplug the flexible cable from J1 on the FRONT unit to separate the chassis.
- ② Take off the flexible cable in the direction of the arrow.
- ③ Unscrew 8 screws Ⓕ (2 × 3 mm, black) to separate the shield plate.

3 Removing the MAIN unit



- ① Unsolder 2 points Ⓖ.
- ② Unscrew 2 nuts Ⓗ.
- ③ Unscrew 6 screws ⓘ (2 × 4 mm, silver), and 2 screws ⓙ (2 × 4 mm, black) from the MAIN unit.
- ④ Take off the MAIN unit in the direction of the arrow.

4 Removing the FRONT unit



- ① Unplug the LCD flexible cable from J2 on the FRONT unit to separate the front panel.
- ② Unscrew 6 screws Ⓚ (2 × 3.5 mm, silver) from the FRONT unit.
- ③ Unsolder the leads of speaker.

SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT

The antenna switching circuit functions as a low-pass filter while receiving and a resonator circuit while transmitting. This circuit does not allow transmit signals to enter the receiver circuits.

Received signals enter the antenna connector (CHASSIS; MP44) and pass through the low-pass filter (L1–L3, C1–C3, C416–C419). The filtered signals are passed through the $\lambda/4$ type antenna switching circuit (D25, L39, D24) and then applied to the RF circuit.

4-1-2 RF CIRCUIT

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

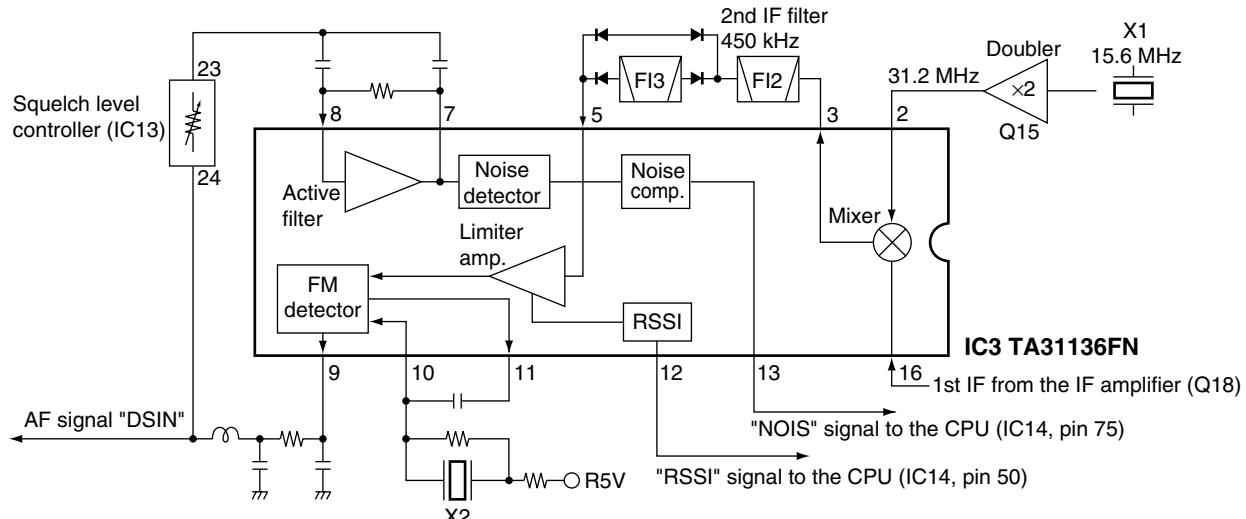
The signals from the antenna switching circuit pass through the two-stage tunable bandpass filters (D21, D20, L38, L37). The filtered signals are amplified at the RF amplifier (Q20) and then passed through the another two-stage tunable bandpass filters (D19, D18, L36, L33) to suppress unwanted signals. The filtered signals are applied to the 1st mixer circuit.

D18–D21 employ varactor diodes, that are controlled by the CPU via the D/A converter (IC27), to track the bandpass filter. These varactor diodes tune the center frequency of an RF pass band for wide bandwidth receiving and good image response rejection.

4-1-3 1ST MIXER AND 1ST IF CIRCUITS

The 1st mixer circuit converts the received signal into fixed frequency of the 1st IF signal with the PLL output frequency. By changing the PLL frequency, only the desired frequency passes through a cristal filter at the next stage of the 1st mixer.

• 2nd IF and demodulator circuits



The RF signals from the bandpass filter are mixed with the 1st LO signals, where come from the RX VCO circuit via the attenuator (R360–R358), at the 1st mixer circuit (Q19) to produce a 31.65 MHz 1st IF signal. The 1st IF signal is passed through a monolithic filter (FI1) in order to obtain selection capability and to pass only the desired signals. The filtered signal is applied to the 2nd IF circuit after being amplified at the 1st IF amplifier (Q18).

4-1-4 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal into a 2nd IF signal. The double-conversion superheterodyne system (which convert receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

The 1st IF signal from the IF amplifier (Q18) is applied to the 2nd mixer section of the FM IF IC (IC3, pin 16), and is mixed with the 2nd LO signal to be converted into a 450 kHz 2nd IF signal.

The FM IF IC (IC3) contains the 2nd mixer, 2nd local oscillator, limiter amplifier, quadrature detector, active filter and noise amplifier circuits. A 2nd LO signal (31.2 MHz) is produced at the PLL circuit by doubling it's reference frequency (15.6 MHz).

The 2nd IF signal from the 2nd mixer (IC3, pin 3) passes through the ceramic filters (FI2, FI3) during narrow channel spacing selection or FI2 only (bypassing FI3) during wide channel spacing selection to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier section (IC3, pin 5) and applied to the quadrature detector section (IC3, pins 10, 11) to demodulate the 2nd IF signal into AF signals.

The demodulated AF signals are output from pin 9 (IC3) and applied to the AF circuit via the receiver mute circuit.

4-1-5 AF AMPLIFIER CIRCUIT

The AF amplifier circuit amplifies the demodulated AF signals to drive a speaker.

The AF signals from the FM IF IC (IC3, pin 9) are amplified at the AF amplifier section of the compander IC (IC9, pins 5, 4) and are then applied to the high-pass filter circuit (IC7a).

The high-pass filter characteristics are controlled by the FSW signal from the I/O expander IC (IC23, pin 14). When FSW signal is high, the cut-off frequency is shifted higher to remove CTCSS or DTCS signals.

The filtered AF signals from the high-pass filter (IC7a, pin 1) are applied to the de-emphasis section of compander IC (IC9, pin 3) with frequency characteristics of -6 dB/octave, and are then passed through the low-pass filter, high-pass filter, expander sections of compander IC (IC9). The output signal from IC9 (pin 38) is applied to the electronic volume controller (IC13, pin 1).

The output AF signals from the electronic volume controller (IC13, pin 2) are applied to the AF power amplifier (IC5) to drive the speaker.

4-1-6 RECEIVE MUTE CIRCUITS

• NOISE SQUELCH

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

Some noise components in the AF signals from the FM IF IC (IC3, pin 9) are passed through the level controller (IC13, pins 24, 23). The level controlled signals are applied to the active filter section in the FM IF IC (IC3, pin 8). Noise components about 10 kHz are amplified and output from pin 7.

The filtered signals are converted into the pulse-type signals at the noise detector section and output from pin 13 (NOIS).

The NOIS signal from the FM IF IC is applied to the CPU (IC14, pin 75). Then the CPU analyzes the noise condition and controls the AF mute signal via "AFMT" line (IC23, pin 13) to the AF regulator (Q23, Q24).

• CTCSS AND DTCS

The tone squelch circuit detects AF signals and opens the squelch only when receiving a signal containing a matching subaudible tone (CTCSS or DTCS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

A portion of the AF signals from the FM IF IC (IC3, pin 9) passes through the low-pass filter (IC20b/a) to remove AF (voice) signals and is applied to the CTCSS or DTCS decoder inside of the CPU (IC14, pin 46) via the "RXDT" line to control the AF mute switch via the I/O expander IC (IC23).

4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT

The microphone amplifier circuit amplifies audio signals within +6 dB/octave pre-emphasis characteristics from the microphone to a level needed for the modulation circuit.

The AF signals (MIC+) from the FRONT unit via J3 (pin 22) are passed through the internal/external microphone switch (IC19, pins 12, 14) and level controller (IC13, pins 9, 10) to the microphone amplifier circuit.

The AF signals from the level controller (IC13) are applied to the microphone amplifier section of compander IC (IC9, pin 12). The amplified signals are passed through the compressor, low-pass filter and high-pass filter sections of IC9.

The filtered AF signals are amplified at the buffer amplifier (Q47) and pre-emphasized with +6dB/octave at the pre-emphasis circuit (C203, R166), and are then applied to the IDC amplifier section of IC9 (pin 8).

The amplified AF signals are passed through the limitter amplifier and low-pass filter sections of IC9 after being passed through the AF mute switch inside of IC9.

The output signals from pin 6 are passed through the splatter filter (IC7c) and level controller (IC13, pins 21, 22), and are then applied to the modulation circuit (D7).

4-2-2 MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signals.

The AF signals from the level controller (IC13) change the reactance of varactor diode (D7) to modulate the oscillated signal at the TX VCO circuit (Q12, D8, D43–D45). The modulated VCO signal is amplified at the buffer amplifiers (Q8, Q6) and is then applied to the drive amplifier circuit via the T/R switch (D4).

The CTCSS/DTCS signals from the CPU (IC14, pin 44) are passed through the low-pass filter (IC7d), level controller (IC13, pins 12, 11) and mixer circuit (IC7b), and are then applied to the VCO circuit via the splatter filter (IC7c).

4-2-3 DRIVE/POWER AMPLIFIER CIRCUITS

The drive/power amplifier circuits amplify the VCO oscillating signal to an output power level.

The signal from the VCO circuit passes through the T/R switch (D4), and is amplified at the YGR (Q3), drive (Q2), power (Q1) amplifiers to obtain 5 W of RF power (at 7.2 V DC).

The amplified signal is passed through the APC detector, antenna switching circuit (D1) and low-pass filter, and is then applied to the antenna connector.

The bias current of the drive (Q2) and power (Q1) amplifiers is controlled by the APC circuit.

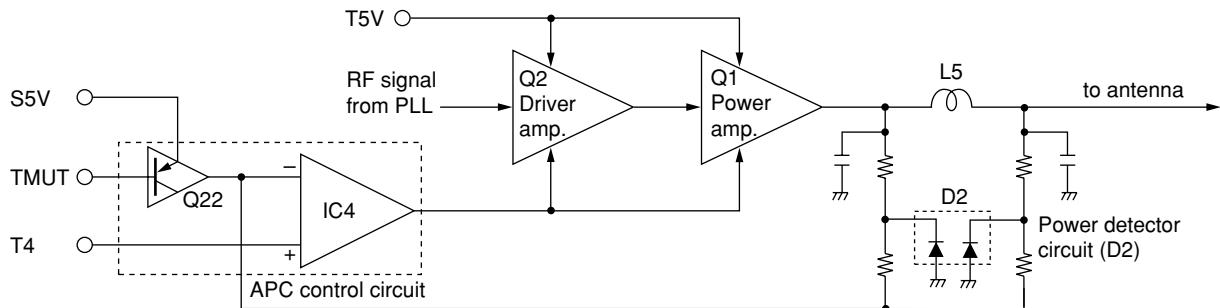
4-2-4 APC CIRCUIT

The APC circuit (IC4, Q22) protects the drive and power amplifiers from excessive current drive, and selects output power of HIGH, LOW2 or LOW1.

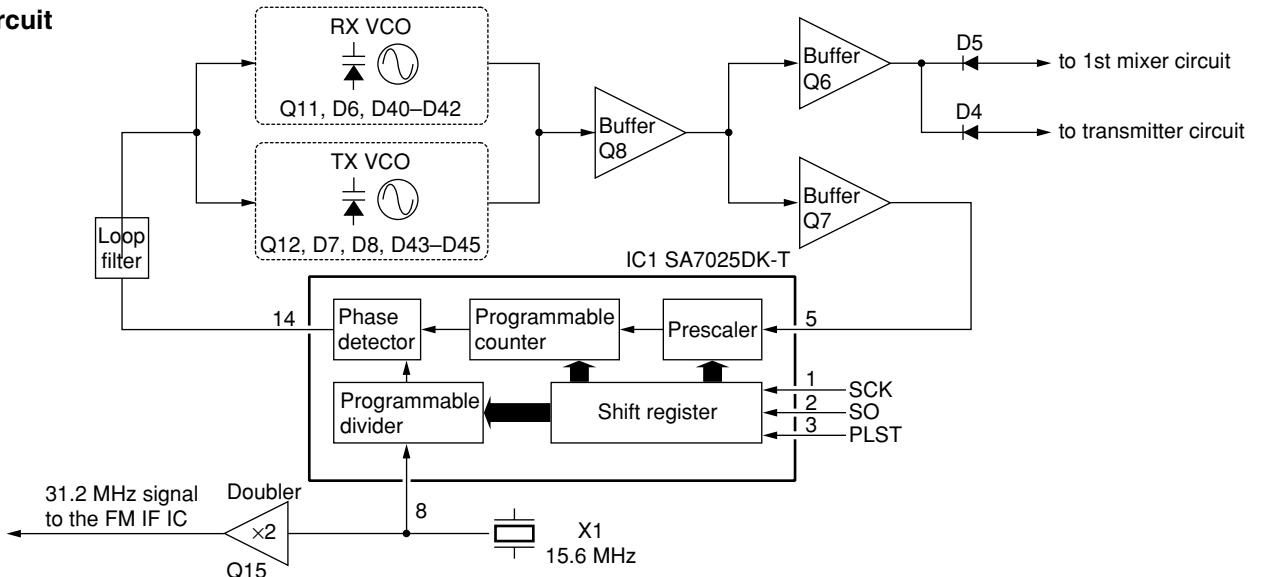
The power detector circuit (D2) detects the transmit power output level and converts it into DC voltage. The output voltage is at a minimum level when the antenna impedance is matched at $50\ \Omega$ and is increased when it is mismatched.

The detected voltage is applied to the differential amplifier (IC4, pin 3), and the "T4" signal from the D/A converter (IC27, pin 4), controlled by the CPU (IC14), is applied to the other input for reference. When antenna impedance is mismatched, the detected voltage exceeds the power setting voltage. Then the output voltage of the differential amplifier (IC4, pin 4) controls the input current of the drive amplifier (Q2) and power amplifier (Q1) to reduce the output power.

• APC circuit



• PLL circuit



4-3 PLL CIRCUITS

4-3-1 PLL CIRCUIT

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

The PLL circuit contains the TX/RX VCO circuit (Q12, Q11). The oscillated signal is amplified at the buffer amplifiers (Q8, Q7) and then applied to the PLL IC (IC1, pin 5).

The PLL IC contains a prescaler, programmable counter, programmable divider and phase detector, etc. The entered signal is divided at the prescaler and programmable counter section by the N-data ratio from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency.

If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

4-3-2 VCO CIRCUIT

The VCO circuit contains a separate RX VCO (Q11, D6, D40-D42) and TX VCO (Q12, D7, D8, D43-D45). The oscillated signal is amplified at the buffer amplifiers (Q8, Q6) and is then applied to the T/R switch (D5, D4). Then the receive 1st LO (Rx) signal is applied to the 1st mixer (Q19) and the transmit (Tx) signal to the YGR amplifier circuit (Q3).

A portion of the signal from the buffer amplifier (Q8) is fed back to the PLL IC (IC1, pin 5) via the buffer amplifier (Q7) as the comparison signal.

4-4 FFSK CIRCUIT DESCRIPTION

4-4-1 GENERAL

IC9 is the compounder IC which is controlled by serial data bus line ("TRD", "MSKE", "DIN", "SCK", "APST", "REGS1", "REGS2", "RTM", "RDT", "FCLR" signals) from the CPU. The IC is composed of FFSK transmitting and receiving circuits, data register circuits, transmitting and receiving data buffer circuits, and so on.

X4 is oscillated 3.58 MHz reference signal to the IC9.

In case of the FFSK signal is used for the PM modulation, the FM/PM switch (IC29) is changed to pin 3.

In case of the FFSK signal is used for the FM modulation, the FM/PM switch (IC29) is changed to pin 5.

The output signal from IC29, pin 4 is applied to the the buffer amplifier (IC7, pins 8, 10), and is applied to the D/A convertor IC (IC13, pins 21, 22). The signal is applied to the modulation circuit (Q12, D7, D8, D43–D45).

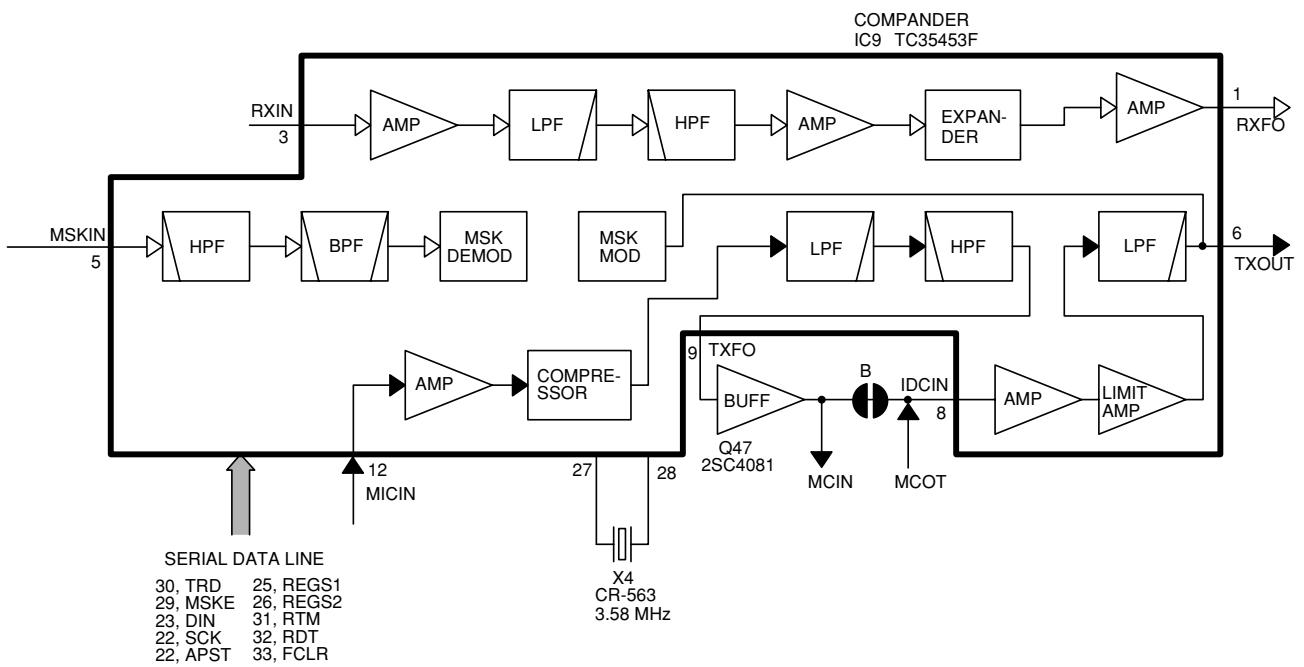
4-4-2 DECODEING CIRCUIT

The input signal from the FM IC (IC3, pin 9) via the "DSIN" signal is applied to the compounder IC (IC9, pin 5), and is then detected bit synchronization detection within 16 bit.

4-4-3 ENCODEING CIRCUIT

The FFSK signal is made by serial data bus line signals, and is then output from the compounder IC (IC9, pin 6).

• Compounder IC block diagram



4-5 POWER SUPPLY CIRCUIT VOLTAGE LINE

LINE	DESCRIPTION
HV	The voltage from the attached battery pack.
VCC	The same voltage as the HV line (battery voltage) which is controlled by the power switch ([VOL] control).
CPU5V	Common 5 V converted from the VCC line by the reference regulator circuit (IC12). The output voltage is applied to the CPU (IC14), 5 V regulator circuit (Q32, Q33) and reset circuit (IC15), and etc.
+5V	Common 5 V converted from the VCC line by the +5V regulator circuit (Q32, Q33).
S5V	Common 5 V converted from the +5V line by the S5V regulator circuit (Q31).
T5V	5 V for transmitter circuits regulated by the T5V regulator circuit (Q29).
R5V	5 V for receiver circuits regulated by the R5V regulator circuit (Q30).

4-6 PORT ALLOCATIONS

4-6-1 CPU (IC14)

Pin number	Port name	Description
4	RESB	Outputs reset signal for the expander IC (IC23).
5	RMUT	Input port for AF mute signal from the optional units via J1 or J2.
6	MMUT	Input port for MIC mute signal from the optional units via J1 or J2.
7	PTOT	Input port for the [PTT] switch Low : While [PTT] switch is pushed.
13	EXST	Outputs strobe signals to the expander IC (IC23).
15	APST	Outputs strobe signals to the compander IC (IC9).
16	DIN	Outputs serial data signals to the compander IC (IC9).
17, 18, 19	RGS1, RGS2, MSKE	Output control signal for the compander IC (IC9).
21	FCLR	Outputs reset signal for the compander IC (IC9).
22– 25	CB10– CB13	Input ports for rotary selector [SEL].
26	VCOS	Outputs TX VCO/RX VCO switching signal for the VCO switch (Q9, Q10). High : While transmitting
28	PLST	Outputs strobe signals to the PLL IC (IC1).
29	ULCK	Input port for the PLL unlock signal. Low : PLL is unlocked.
34	SCK	Outputs clock signal for the PLL IC (IC1), compander IC (IC9), expander IC (IC23), D/A converter (IC13), etc.

Pin number	Port name	Description
35	SO	Outputs data signals for the PLL IC (IC1), compander IC (IC9), expander IC (IC23), D/A converter (IC13), etc.
36	DAST	Outputs strobe signals to the D/A converter (IC13).
39	DTAC	Output clock signal to the DTMF decoder (IC17).
43	SENC	Outputs single tone signal.
44	CTDA	Outputs CTCSS/DTCS tone signal.
45	SDEC	Single tone signal input port for decoding.
46	RXDT	CTCSS/DTCS signals input port for decoding.
47	AFVI	Input port for the volume control [VOL]. High : [VOL] is maximum clockwise.
49	LVIN	Input port for the PLL lock voltage.
50	RSSI	Input port for the RSSI detection.
59	RES	Input port for the reset signal.
68	DTSD	Outputs serial data signals to the DTMF decoder IC (IC17).
70	TMUT	Outputs transmit mute signal. Low : During unlock or while muted
71	R5C	Outputs R5 regulator control signal. Low: While receiving
73	T5C	Outputs T5 regulator control signal. Low: While transmitting
75	NOIS	Input port for noise signals (pulse-type) for noise squelch operation.
81	SDA	I/O port for data signals from/to the D/A converter (IC27).
82	MSO	I/O port for data signals from/to EEPROMs (IC16, IC24).
87	BEEP	Outputs beep audio signals.
94	MSCK	Outputs clock signal to EEPROMs (IC16, IC24).
95	SCL	Outputs clock signal to the D/A converter (IC27).

4-6-2 I/O EXPANDER (IC23)

Pin number	Port name	Description
4	BUSY	Outputs BUSY detection. Low : The channel is busy.
6	DUSE	Outputs low-pass filter cut-off frequency control signal when DTCS is activated.
7	W/N	Outputs IF bandwidth control signal. High : While IF bandwidth is narrow.
11	S5C	Outputs S5 regulator control signal.
12	SPCN	Outputs internal speaker select signal.
13	AFMT	Outputs control signal for the AF amplifier regulator circuit. High: While AF amp. is activated.
14	FSW	Outputs high-pass filter's characteristics select signal.

SECTION 5 ADJUSTMENT PROCEDURES

5-1 PREPARATION

When you adjust the contents on pages 5-5 and 5-6, SOFTWARE ADJUSTMENT, the optional CS-F30G ADJ ADJUSTMENT SOFTWARE (Rev. 1.0 or later), *OPC-966 JIG CABLE (modified OPC-966 CLONING CABLE) are required.

■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 7.5 V DC Current capacity : 5 A or more	Audio generator	Frequency range : 300–3000 Hz Output level : 1–500 mV
FM deviation meter	Frequency range : DC–300 MHz Measuring range : 0 to ±10 kHz	Attenuator	Power attenuation : 40 or 50 dB Capacity : 10 W or more
Frequency counter	Frequency range : 0.1–300 MHz Frequency accuracy : ±1 ppm or better Sensitivity : 100 mV or better	Standard signal generator (SSG)	Frequency range : 100–300 MHz Output level : 0.1 µV–32 mV (−127 to −17 dBm)
Digital multimeter	Input impedance : 10 MΩ/V DC or better	DC voltmeter	Input impedance : 50 kΩ/V DC or better
RF power meter (terminated type)	Measuring range : 1–10 W Frequency range : 100–300 MHz Impedance : 50 Ω SWR : Less than 1.2 : 1	Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–20 V
		AC millivoltmeter	Measuring range : 10 mV–10 V

■ SYSTEM REQUIREMENTS

- IBM PC compatible computer with an RS -232C serial port (38400 bps or faster).
- Microsoft Windows 95 or Windows 98
- Intel i486DX processor or faster (Pentium 100 MHz or faster recommended)
- At least 16 MB RAM and 10 MB of hard disk space
- 640×480 pixel display (800×600 pixel display recommended)

■ ADJUSTMENT SOFTWARE INSTALLATION

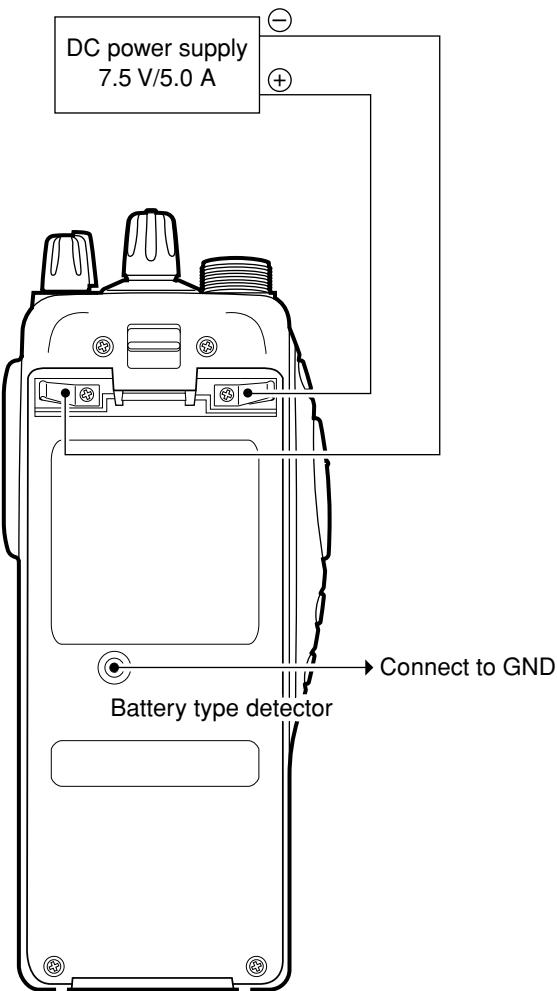
- ① Boot up Windows.
- Quit all applications when Windows is running.
- ② Insert the 'CS-F30G' into the appropriate drive.
- ③ Select 'Run' from the [Start] menu.
- ④ Type the setup program name using the full path name, then push [Enter] key.
(ex. D:\CSF30GADJ\disk1\Setup.exe)
- ⑤ Follow the prompts.
- ⑥ Program group 'CS-F30G ADJ' appears in the 'Programs' folder of the [Start] menu.

■ STARTING SOFTWARE ADJUSTMENT

- ① Connect IC-F30GT, F30GS, F31GT or F31GS and PC with *OPC-966 JIG CABLE.
- ② Turn the transceiver power ON.
- ③ Boot up Windows, and click the program group 'CS-F30G ADJ' in the 'Programs' folder of the [Start] menu, then CS-F30G ADJ's window appears.
- ④ Click 'Connect' on the CS-F30G's window, then appears IC-F30GT, F30GS, F31GT or F31GS's up-to-date condition.
- ⑤ Set or modify adjustment data as desired.

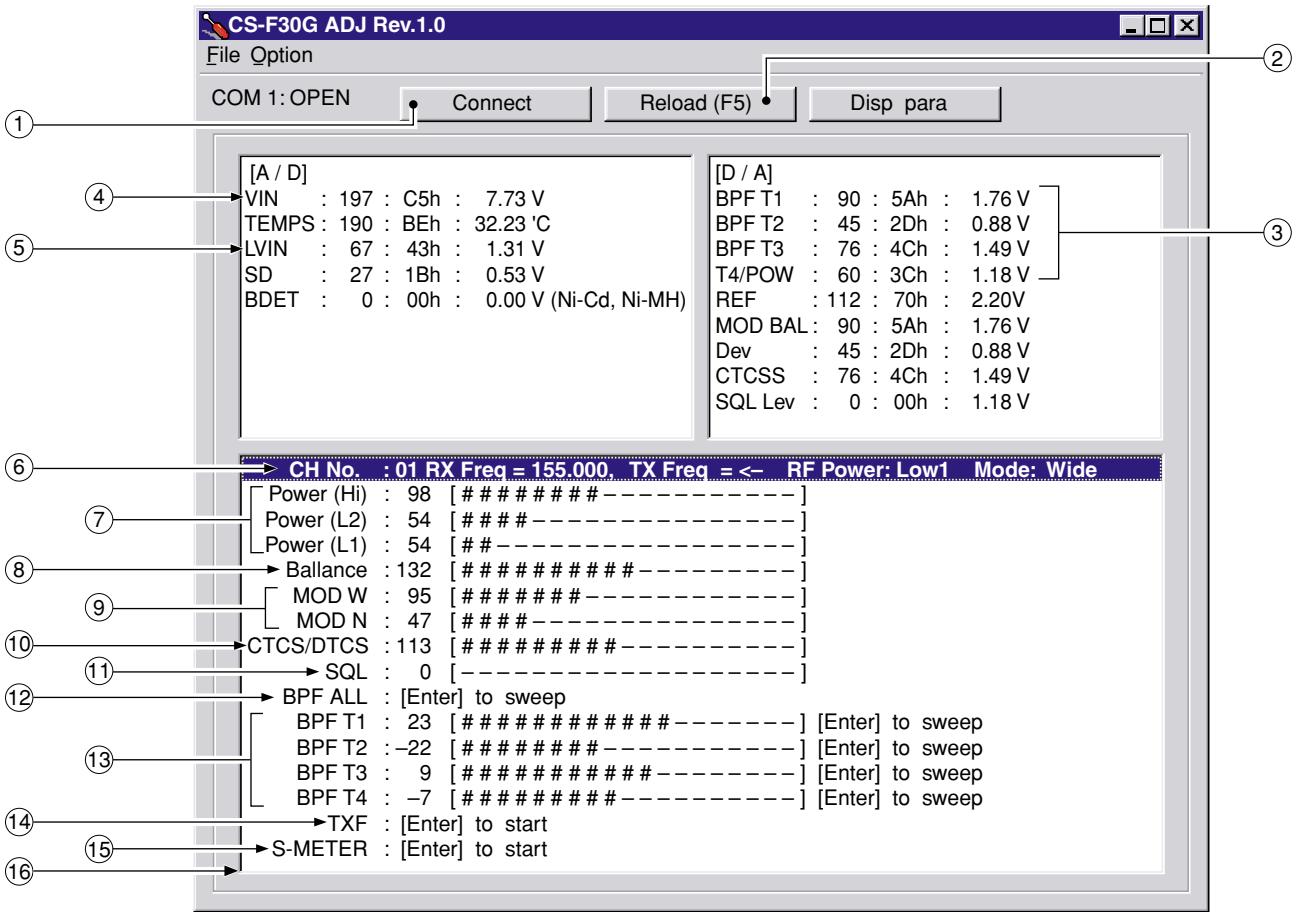
• High power transmission

When you adjust the output power (high power), the battery type detector must be connected to GND (see illustration at below). Otherwise the transceiver does not transmit high power, the output power will be low.



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Screen shots produced with permission from Microsoft Corporation. All other products or brands are registered trademarks or trademarks of their respective holders.

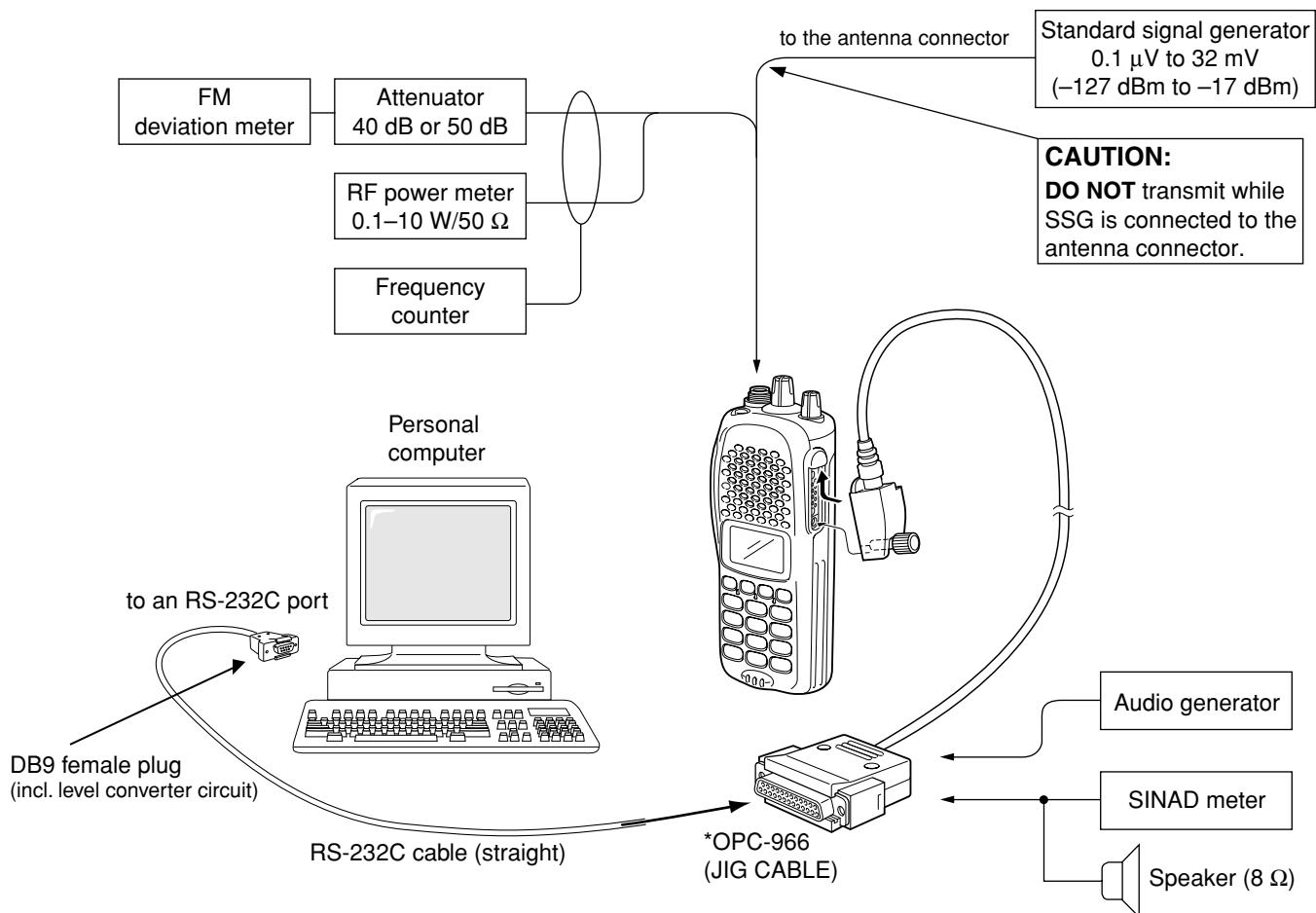
- Screen display example



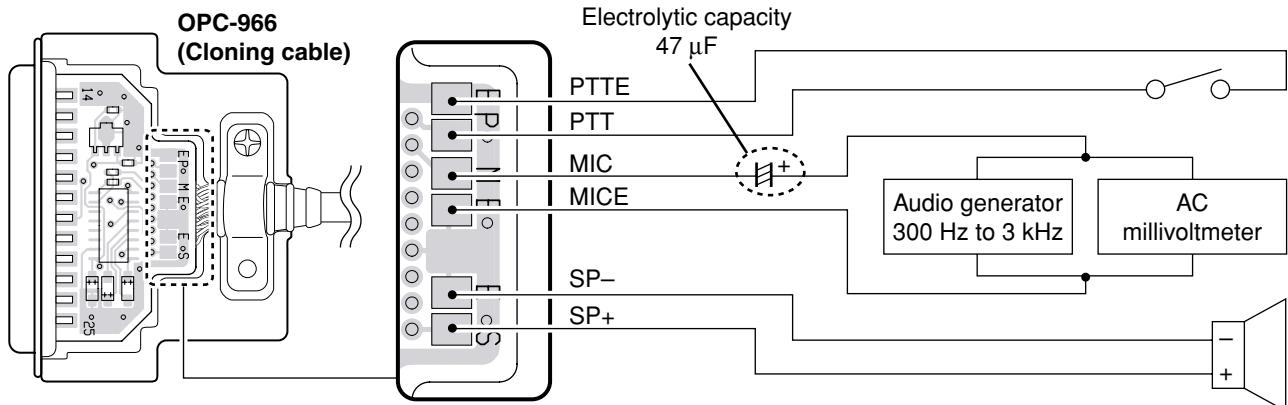
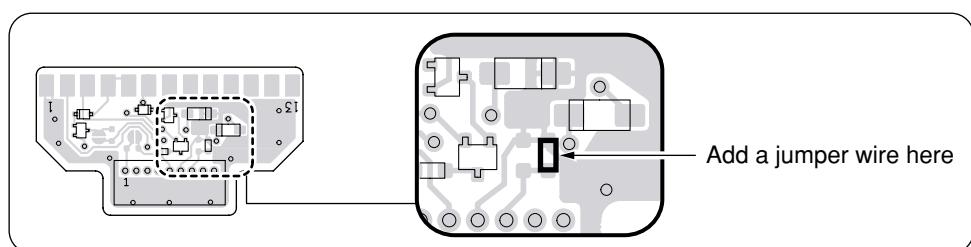
NOTE: The above values for settings are example only.
Each transceiver has its own specific values for each setting.

- | | |
|---------------------------------------|--|
| (1) : Transceiver's connection state | (9) : FM deviation |
| (2) : Reload adjustment data | (10) : CTCSS/DTCS deviation |
| (3) : Receive sensitivity measurement | (11) : Squelch level |
| (4) : Connected DC voltage | (12) : Receive sensitivity (automatically) |
| (5) : PLL lock voltage | (13) : Receive sensitivity (manually) |
| (6) : Operating channel select | (14) : Reference frequency |
| (7) : RF output power | (15) : S-meter |
| (8) : Modulation balance | (16) : Adjustment items |

• Connection



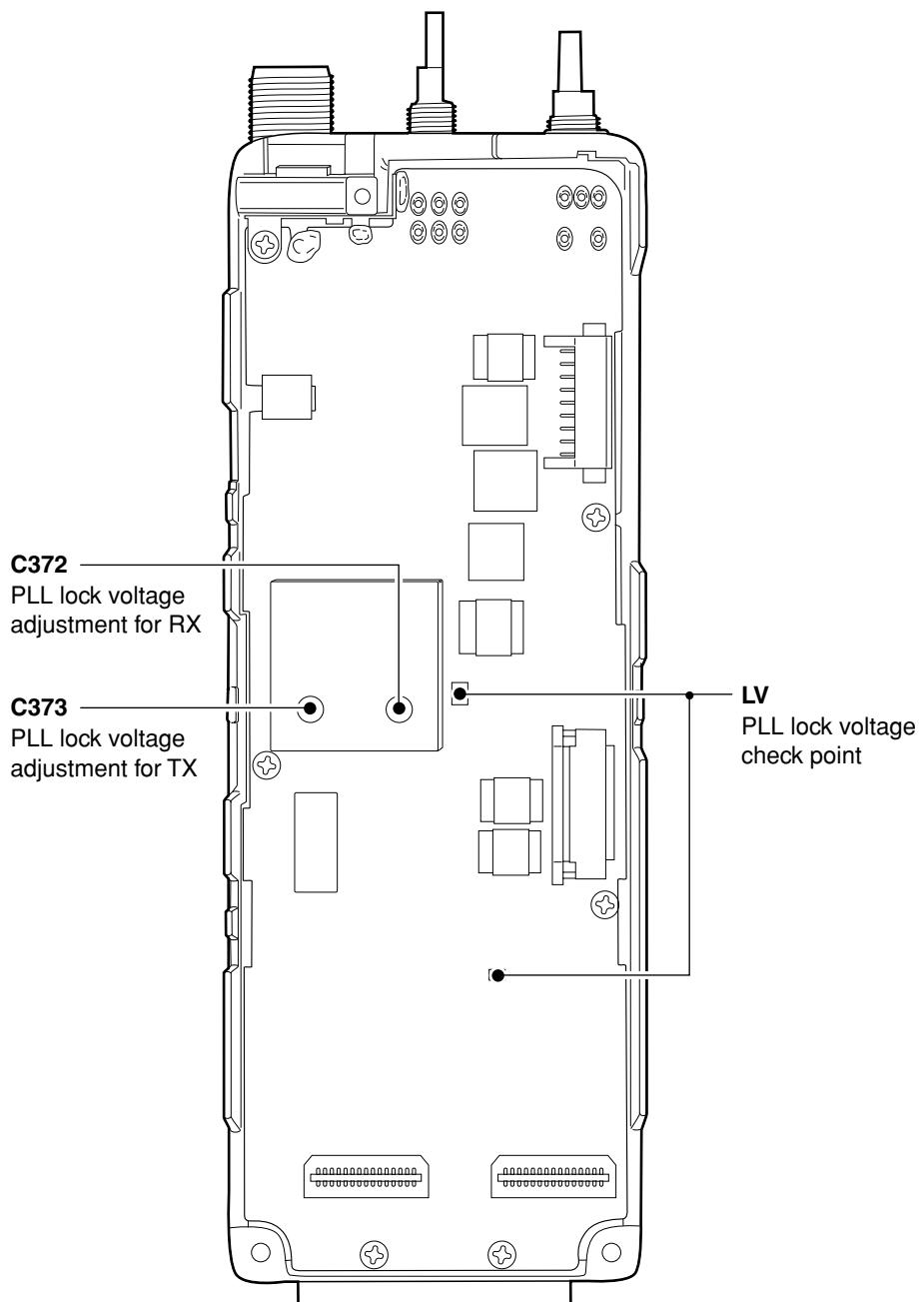
• *OPC-966 (JIG CABLE)



5-2 PLL ADJUSTMENT

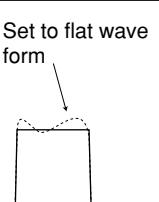
ADJUSTMENT		ADJUSTMENT CONDITIONS	MEASUREMENT		VALUE	ADJUSTMENT	
			UNIT	LOCATION		UNIT	ADJUST
PLL LOCK VOLTAGE	1	• Operating freq. : 136.000 MHz • Receiving	MAIN	Connect a digital multimeter or an oscilloscope to the check point, "LV".	1.2 V	MAIN	C372
	2	• Transmitting			1.0 V		C373
	3	• Operating freq. : 174.000 MHz • Receiving			3.0–4.5 V		Verify
	4	• Transmitting					

- MAIN unit



5-3 SOFTWARE ADJUSTMENT

Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard.

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE
			UNIT	LOCATION	
REFERENCE FREQUENCY [TXF]	1	<ul style="list-style-type: none"> • Operating freq. : 174.000 MHz • Output power : Low1 • Connect an RF power meter or 50 Ω dummy load to the antenna connector. • Transmitting 	Top panel	Loosely couple a frequency counter to the antenna connector.	174.0000 MHz
OUTPUT POWER [Power (Hi)]	1	<ul style="list-style-type: none"> • Operating freq. : 136.000 MHz • Output power : High • Transmitting 	Top panel	Connect an RF power meter to the antenna connector.	5.0 W
[Power (L2)]	2	<ul style="list-style-type: none"> • Output power : Low2 • Transmitting 			2.0 W
[Power (L1)]	3	<ul style="list-style-type: none"> • Output power : Low1 • Transmitting 			1.0 W
MODULATION BALANCE [Ballance]	1	<ul style="list-style-type: none"> • Operating freq. : 155.000 MHz • Output power : Low1 • Set an FM deviation meter as: <ul style="list-style-type: none"> HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P-P)/2 • Push [P0] key while transmitting 	Top panel	Connect an FM deviation meter with an oscilloscope to the antenna connector through an attenuator.	
FM DEVIATION [MOD W]	1	<ul style="list-style-type: none"> • Operating freq. : 155.000 MHz • Output power : Low1 • IF bandwidth : Wide • Set the FM deviation meter as: <ul style="list-style-type: none"> HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P-P)/2 • Connect the audio generator to the multi connector through the JIG cable (*OPC-966) and set as : 1.0 kHz/150 mVrms • Transmitting 	Top panel	Connect an FM deviation meter to the antenna connector through the attenuator.	$\pm 4.1 \text{ kHz } \textcircled{A}$ $\pm 3.1 \text{ kHz } \textcircled{B}$
[MOD N]	2	<ul style="list-style-type: none"> • IF bandwidth : Narrow • Transmitting 			$\pm 2.1 \text{ kHz}$
CTCSS/DTCS DEVIATION [CTCS/DTCS]	1	<ul style="list-style-type: none"> • Operating freq. : 155.000 MHz • Output power : Low1 • IF bandwidth : Wide • CTCSS : 88.5 Hz • DTCS code : 007 • No audio applied to the [MIC] input. • Transmitting 	Top panel	Connect an FM deviation meter to the antenna connector through the attenuator.	$\pm 0.70 \text{ kHz } \textcircled{1}$ $\pm 0.56 \text{ kHz } \textcircled{2}$

(A): W/N version, (B): M/N version

SOFTWARE ADJUSTMENT – continued

Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard.

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE
		UNIT	LOCATION	
RX SENSITIVITY [BPF T1] – [BPF T4]	1 <ul style="list-style-type: none"> • Operating freq. : 136.000 MHz • IF bandwidth : Wide • Connect a standard signal generator to the antenna connector and set as: <ul style="list-style-type: none"> Frequency : 136.000 MHz Level : 10 µV* (-87 dBm) Modulation : 1 kHz Deviation : ±3.5 kHz (A) ±2.8 kHz (B) • Receiving CONVENIENT: <ul style="list-style-type: none"> The BPF T1–BPF T4 can be adjusted automatically. ①-1: Set the cursol to “BPF ALL” on the adjustment program and then push [ENTER] key. ①-2: The connected PC tunes BPF T1–BPF T4 to peak levels. or ②-1: Set the cursol to one of BPF T1, T2, T3, or T4 as desired. ②-2: Push [ENTER] key to start tuning. ②-3: Repeat ②-1 and ②-2 to perform additional BPF tuning. 	MAIN	Connect a SINAD meter with an 8 Ω load to the multi connector through the JIG cable (see page 5-3).	Minimum distortion level
S-METER [S-METER]	1 <ul style="list-style-type: none"> • Operating freq. : 136.000 MHz • IF bandwidth : Wide • Connect an SSG to the antenna connector and set as: <ul style="list-style-type: none"> Frequency : 136.000 MHz Level : 14 µV* (-84 dBm) Modulation : 1 kHz Deviation : ±3.5 kHz (A) ±2.8 kHz (B) • Receiving 		Push [ENTER] key on the connected computer keyboard to set “S3 level”.	
	2 <ul style="list-style-type: none"> • Set an SSG as : <ul style="list-style-type: none"> Level : 0.45 µV* (-114 dBm) Modulation : 1 kHz Deviation : ±3.5 kHz (A) ±2.8 kHz (B) • Receiving 		Push [ENTER] key on the connected computer keyboard to set “S1 level”.	
SQUELCH LEVEL [SQL]	1 <ul style="list-style-type: none"> • Operating freq. : 155.000 MHz • IF bandwidth : Wide • Connect an SSG to the antenna connector and set as: <ul style="list-style-type: none"> Frequency : 155.000 MHz Level : 0.2 µV* (-121 dBm) Modulation : 1 kHz Deviation : ±3.5 kHz (A) ±2.8 kHz (B) • Receiving 	Front panel	Internal speaker	Set “SQL level” to close squelch. Then set “SQL level” at the point where the audio signals just appears.

*The output level of the standard signal generator (SSG) is indicated as the SSG's open circuit.

(A): W/N version, (B): M/N version

SECTION 6 PARTS LIST

[FRONT UNIT]

REF NO.	ORDER NO.	DESCRIPTION		M.
IC1	1130009860	S.IC	TC74VHC373FT (EL)	T
IC2	1110002750	S.IC	TA75S01F (TE85R)	T
Q1	1530002850	S.TRANSISTOR	2SC4116-BL (TE85R)	T
Q2	1530002850	S.TRANSISTOR	2SC4116-BL (TE85R)	T
Q3	1590002150	S.TRANSISTOR	DTC144TE TL	T
Q4	1590002150	S.TRANSISTOR	DTC144TE TL	T
Q5	1590002150	S.TRANSISTOR	DTC144TE TL	T
Q6	1560001130	S.FET	CPH3403-TL	T
Q7	1560001130	S.FET	CPH3403-TL	T
Q8	1530002060	S.TRANSISTOR	2SC4081 T106 R	T
Q9	1590000430	S.TRANSISTOR	DTC144EUA T106	T
D1	1790001280	S.DIODE	MA111 (TX)	T
D2	1790001280	S.DIODE	MA111 (TX)	T
D3	1790001200	S.DIODE	MA6S121 (TX)	T
D4	1790001280	S.DIODE	MA111 (TX)	T
R1	7030007300	S.RESISTOR	ERJ2GEJ 332 X (3.3 kΩ)	T
R2	7030005030	S.RESISTOR	ERJ2GEJ 152 X (1.5 kΩ)	T
R3	7030007250	S.RESISTOR	ERJ2GEJ 220 X (22 Ω)	T
R4	7030009150	S.RESISTOR	ERJ2GEJ 824 X (820 kΩ)	T
R5	7030009150	S.RESISTOR	ERJ2GEJ 824 X (820 kΩ)	T
R6	7030006610	S.RESISTOR	ERJ2GEJ 394 X (390 kΩ)	T
R7	7030008310	S.RESISTOR	ERJ2GEJ 564 X (560 kΩ)	T
R8	7030008370	S.RESISTOR	ERJ2GEJ 561 X (560 Ω)	T
R9	7030004990	S.RESISTOR	ERJ2GEJ 221 X (220 Ω)	T
R10	7030005030	S.RESISTOR	ERJ2GEJ 152 X (1.5 kΩ)	T
R11	7030007300	S.RESISTOR	ERJ2GEJ 332 X (3.3 kΩ)	T
R12	7030005060	S.RESISTOR	ERJ2GEJ 333 X (33 kΩ)	T
R13	7030007280	S.RESISTOR	ERJ2GEJ 331 X (330 Ω)	T
R14	7030005090	S.RESISTOR	ERJ2GEJ 104 X (100 kΩ)	T
R17	7030005090	S.RESISTOR	ERJ2GEJ 104 X (100 kΩ)	T
R18	7410000750	S.ARRAY	EXB-V4V 104JV (100 kΩ)	T
R20	7030005170	S.RESISTOR	ERJ2GEJ 474 X (470 kΩ)	T
R21	7030005090	S.RESISTOR	ERJ2GEJ 104 X (100 kΩ)	T
R22	7030005170	S.RESISTOR	ERJ2GEJ 474 X (470 kΩ)	T
R23	7030005050	S.RESISTOR	ERJ2GEJ 103 X (10 kΩ)	T
R24	7030005240	S.RESISTOR	ERJ2GEJ 473 X (47 kΩ)	T
R25	7030008300	S.RESISTOR	ERJ2GEJ 184 X (180 kΩ)	T
R26	7030007340	S.RESISTOR	ERJ2GEJ 153 X (15 kΩ)	T
R27	7030008010	S.RESISTOR	ERJ2GEJ 123 X (12 kΩ)	T
C1	4030016930	S.CERAMIC	ECJ0EB1A104K	T
C2	4030016930	S.CERAMIC	ECJ0EB1A104K	T
C3	4030016930	S.CERAMIC	ECJ0EB1A104K	T
C4*	4550006150	S.TANTALUM	ECST1CY105R	T
C6*	4550006150	S.TANTALUM	ECST1CY105R	T
C7*	4550006150	S.TANTALUM	ECST1CY105R	T
C8*	4550006150	S.TANTALUM	ECST1CY105R	T
C9*	4550006150	S.TANTALUM	ECST1CY105R	T
C10*	4550006150	S.TANTALUM	ECST1CY105R	T
C11*	4550006150	S.TANTALUM	ECST1CY105R	T
C12	4030014180	S.CERAMIC	ECUE1H470JCQ	T
C13	4030014180	S.CERAMIC	ECUE1H470JCQ	T
C14	4030014180	S.CERAMIC	ECUE1H470JCQ	T
C15	4030014180	S.CERAMIC	ECUE1H470JCQ	T
C16	4030013850	S.CERAMIC	ECUE1E102KBQ	T
C17	4030014180	S.CERAMIC	ECUE1H470JCQ	T
C18	4030014180	S.CERAMIC	ECUE1H470JCQ	T
C19	4030016930	S.CERAMIC	ECJ0EB1A104K	T
C20	4030014180	S.CERAMIC	ECUE1H470JCQ	T
C21*	4550006150	S.TANTALUM	ECST1CY105R	T
C22	4030016930	S.CERAMIC	ECJ0EB1A104K	T
C23*	4550006150	S.TANTALUM	ECST1CY105R	T
C24	4030016790	S.CERAMIC	ECJ0EB1C103K	T
C25	4030014180	S.CERAMIC	ECUE1H470JCQ	T
C26	4030016930	S.CERAMIC	ECJ0EB1A104K	T
C27	4030017230	S.CERAMIC	ECUE1E271KBQ	T
C28	4030016790	S.CERAMIC	ECJ0EB1C103K	T
C29	4030013850	S.CERAMIC	ECUE1E102KBQ	T
C30	4030016930	S.CERAMIC	ECJ0EB1A104K	T
J1	6510022360	S.CONNECTOR	26FLZ-SM1-TB	T
J2	6510022200	S.CONNECTOR	40FLZ-SM1-R-TB	T

[FRONT UNIT]

REF NO.	ORDER NO.	DESCRIPTION		M.
DS1	5010000160	S.LED	LNJ310M6URA	B
DS2	5010000160	S.LED	LNJ310M6URA	B
DS3	5010000160	S.LED	LNJ310M6URA	B
DS4	5010000160	S.LED	LNJ310M6URA	B
DS5	5040002170	S.LED	LNJ210C6ARA	B
DS6	5010000120	S.LED	LNJ310G-(TR)	[GT] B
DS7	5010000120	S.LED	LNJ310G-(TR)	[GT] B
DS8	5010000120	S.LED	LNJ310G-(TR)	[GT] B
DS9	5010000120	S.LED	LNJ310G-(TR)	[GT] B
DS10	5030001870	LCD	EDMMUD1FA0	B
DS11	5010000120	S.LED	LNJ310G-(TR)	[GT] B
DS12	5010000120	S.LED	LNJ310G-(TR)	[GT] B
DS13	5010000160	S.LED	LNJ310M6URA	B
DS14	5010000120	S.LED	LNJ310G-(TR)	[GS] B
DS15	5010000120	S.LED	LNJ310G-(TR)	[GS] B
MC1	7700002310	MICROPHONE	EM-140	B
S1	2230001060	S.SWITCH	EVQ-PUL 02K	T
S2	2230001060	S.SWITCH	EVQ-PUL 02K	T
S3	2230001060	S.SWITCH	EVQ-PUL 02K	T
S4	2230001060	S.SWITCH	EVQ-PUL 02K	T
S5	2230001060	S.SWITCH	EVQ-PUL 02K	T
SP1*	2510001060	SPEAKER	K036NA500-47	T
W1	7120000470	JUMPER	ERDS2T0	T
W3	7030003860	S.RESISTOR	ERJ3GE JPW V	T
EP1	0910055257	PCB	B 5489G	

[GT]: IC-F30GT/F31GT, [GS]: IC-F30GS/F31GS,
[F30GI]: IC-F30GT/F30GS, [F31GI]: IC-F31GT/F31GS
[IS]: Intrinsically safe version, [BIIS]: BIIS version

M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)
*=safety critical components S.=Surface mount

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION			M.
J3	6510022360	S.CONNECTOR	26FLZ-SM1-TB		T
F1	5210000710 5210000880	S.FUSE S.FUSE	KAB 2402 322 NA29 043403.5NRP	[F31G] [F30G]	T T
S1	2250000180	ENCODER	EC10SP16-47		B
W2	7030003860	S.RESISTOR	ERJ3GE JPW V		B
W3	7030003860	S.RESISTOR	ERJ3GE JPW V		T
W4	7030003860	S.RESISTOR	ERJ3GE JPW V		B
W5	8900009790	CABLE	OPC-972		
EP1	0910055243	PCB	B 5511C		

[GT]: IC-F30GT/F31GT,
 [GS]: IC-F30GS/F31GS,
 [F30G]: IC-F30GT/F30GS,
 [F31G]: IC-F31GT/F31GS
 [IS]: Intrinsically safe version

M.=Mounted side (T: Mounted on the Top side,
 B: Mounted on the Bottom side)
 * =safety critical components
 S.=Surface mount

SECTION 7 MECHANICAL PARTS AND DISASSEMBLY

[CHASSIS PARTS]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
MP1	8210017211	2337 front panel-1 assembly [GT]	1
	8210017350	2337 S-front panel assembly [GS]	1
MP2	8310049450	2337 window plate	1
MP4	8930052850	2337 release button	1
MP5	8930052970	2337 PTT plate	1
MP8	8210017100	2337 rear panel	1
MP9	8210017080	2337 reflector	1
MP10	8930052981	2337 switch plate-1	1
MP12	8010018251	2337 chassis-1	1
MP13	8930052641	2337 key board-1 [GT]	1
	8930059691	2337 key board (A)-1 [GT version BIIS]	1
	8930053170	2337 4-key [GS]	1
MP14	8930053650	2336 main seal	1
MP16	8930052840	2337 T-rubber	1
MP17	8930054540	2336 top key	1
MP18	8930052991	2337 terminal-1	1
MP19	8610010910	Knob N281	1
MP20	8610010920	Knob N282	1
MP21	8510013161	2337 main shield-1	1
MP22	8930053670	2337 side plate	1
MP23	8930053000	2337 window sheet	1
MP25	8510013480	2336 PA shield	1
MP26	8830001480	VR nut (O)	1
MP29	8930053210	2337 microphone sheet	1
MP32	8830001500	2337 nut	1
MP33	8830001511	Nut (I)-1	1
MP34	8810009220	Screw PH B0 M2 × 8 ZK (BT)	2
MP35	8930042080	1922 minus terminal	1
MP37	8950004420	1652 9-pin connector	1
MP40	8810008970	Screw FH BT No.0 M2 × 3.5 NI-ZU	6
MP41	8810009180	Screw FH BT No.0 M2 × 5 NI-ZU	1
MP43	8210017091	2337 terminal holder-1	1
MP44	8950005311	Antenna connector-103-1	1
MP49	8510013220	2337 antenna plate	1
MP50	8930053440	2337 A-PTT plate	1
MP51	8930053431	Sponge (GP)-1	2
MP52	881000100	Screw PH M2 × 4 ZK	2
MP53	8930053630	Seal O-ring (AH)	1
MP54	8930053680	Spring (AG)	1
MP55	8810004890	Screw PH No.0 M2 × 6 ZK	2
MP56	8810005360	Screw PH No.0 M2 × 3 ZK	8
MP57	8810009560	Screw PH BT M2 × 6 ZK	2
MP58	8810005700	Screw PH No.0 M2 × 4 ZK	3
MP59	8810009510	Screw PH BT M2 × 4 NI-ZU	8
MP60	8930046000	1903 microphone sponge	1
MP61	8930053660	2337 side seal	1
MP63	8930053880	2337 key sheet [GT]	1
	8930054010	2337 4-key sheet [GS]	1
MP64	8930051781	Insulation sheet GA-1	1
MP65	8930053890	2337 T-K sheet	1

[GT]: IC-F30GT/F31GT

[GS]: IC-F30GS/F31GS

[FRONT UNIT]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
DS10	5030001870	LCD EDMMUD1FA0	1
SP1*	2510001060	Speaker K036NA500-47	1
MC1	7700002310	Microphone EM-140	1
MP1	8510013230	2337 LOGIC shield	1
MP2	8930053320	2337 LOGIC spring	1

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
MP1	8510013000	2336 VCO case	1
MP2	8510011180	1923 VCO cover	1
MP3	8410002370	2337 PA heat sink (using Q1:2SK2974)	1
MP6	8950005330	2337 9-pin base	1
MP7	8950005320	2337 contact	1
W5	8950009790	Cable OPC-972	1

Screw abbreviations

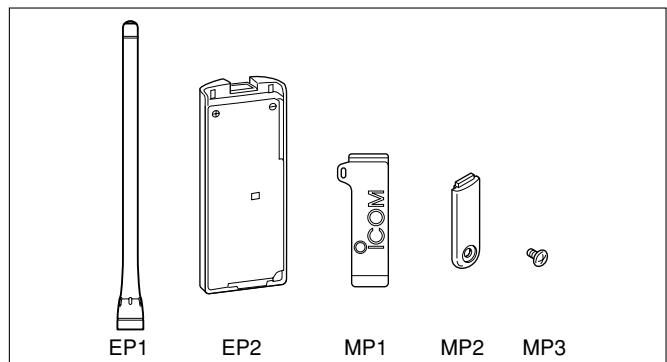
B0, BT: Self-tapping PH: Pan head FH: Flat head

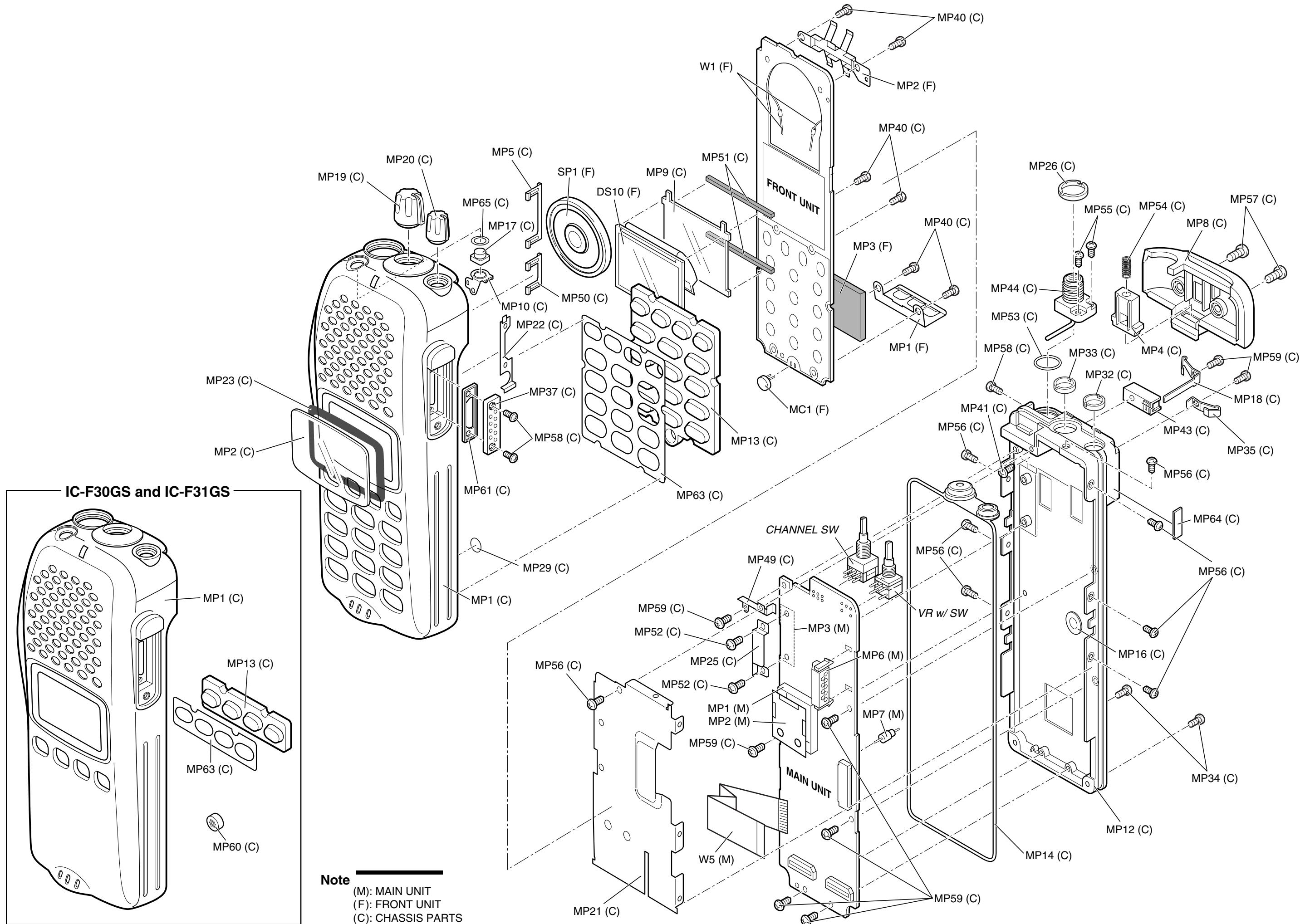
NI-ZU: Nickel-Zinc ZK: Black

[ACCESSORIES]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
EP1	Optional products	Antenna FA-SC55V-1	1
EP2*	Optional products	Battery BP-210FM for intrinsically safe version	1
		Battery BP-210 for other version	1
MP1	8010019360	MB-74N clip	1
MP2	8210017071	2337 C-panel-1	1
MP3	8810003700	ICOM screw B4	1

* : Safety critical components





SECTION 8 SEMI-CONDUCTOR INFORMATION

8 - 1 TRANSISTORS AND FETS

NAME	SYMBOL	INSIDE VIEW
2SA1362 GR	AEG	
2SB1132 R	BARB	
2SC4081 R 2SC4116 GR 2SC4213 B 2SC4215 O 2SC4226 R25	BR LG AB QO R25	
2SK880-Y	XY	
2SK1829	K1	
2SK2973	K1	
2SK2974	K2974	(TOP VIEW)

NAME	SYMBOL	INSIDE VIEW
3SK206-T1 U78 3SK293	U78 UF	
CPH3403-TL	KC	
DTA144EUA	16	
DTC144EUA	26	
DTC144TE TL	06	
UN911H	6P	
XP1214	9H	

NAME	SYMBOL	INSIDE VIEW
XP6501 AB	5N	

8 - 2 DIODES

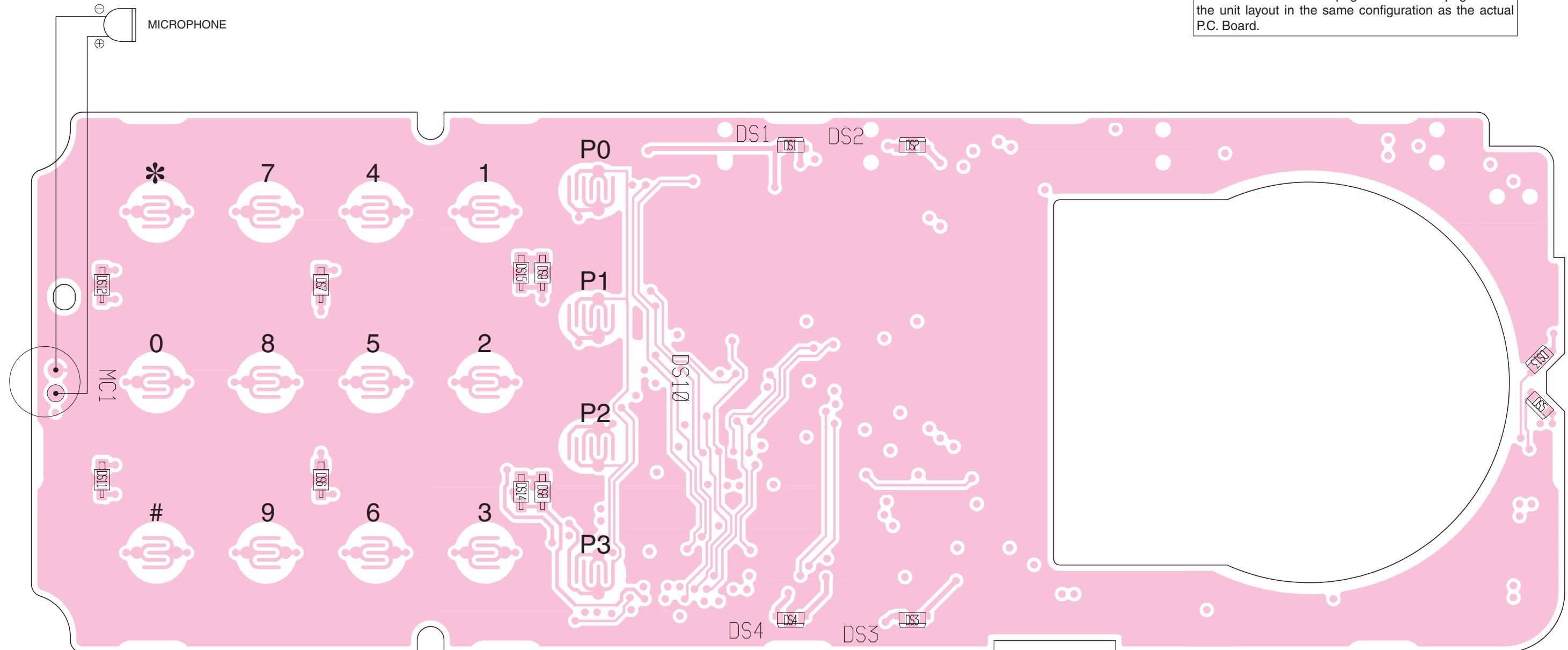
NAME	SYMBOL	INSIDE VIEW
1SV245 HVC350BTRF	T3 BO	
DAN202U	N	
DAP202U	P	
MA111 MA2S111	1B A	
MA77	4B	

NAME	SYMBOL	INSIDE VIEW
MA713	MIN	
MA742	M1U	

SECTION 9 BOARD LAYOUTS

9 - 1 FRONT UNIT

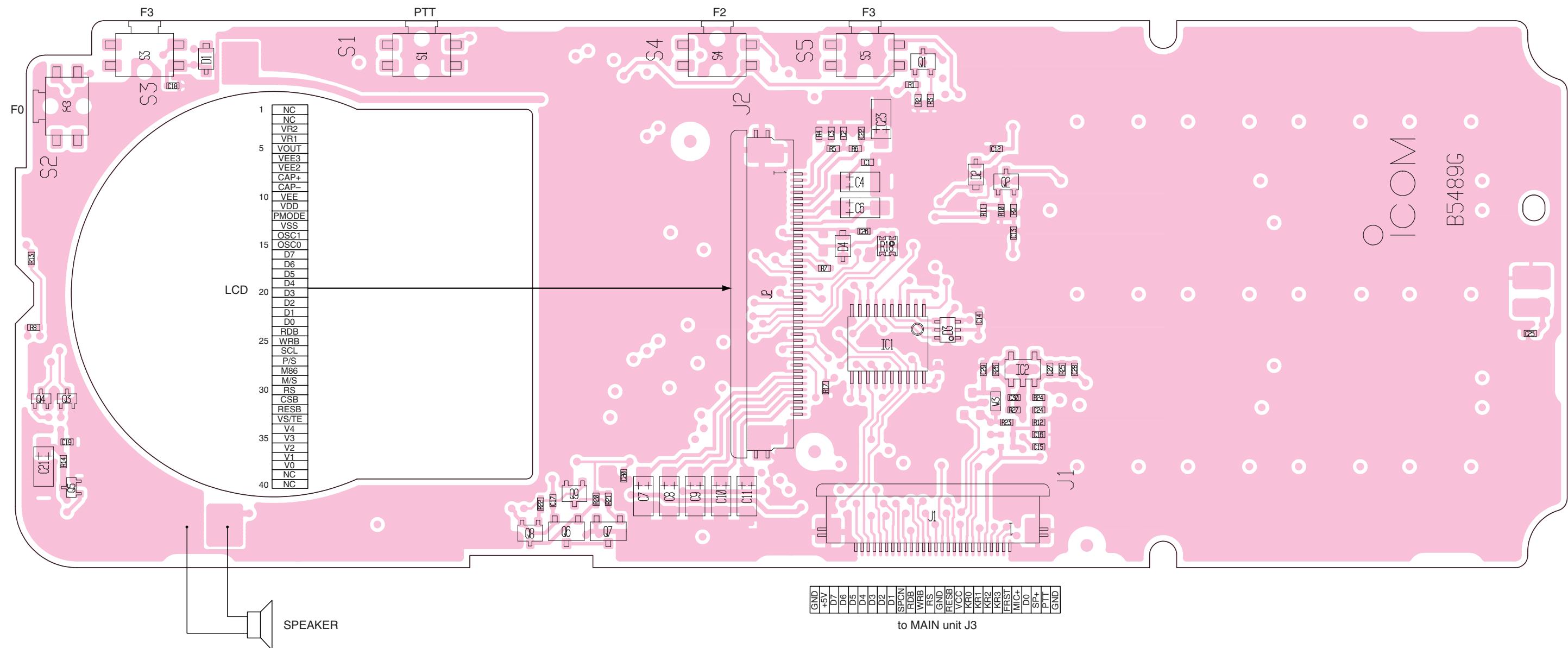
•TOP VIEW



FRONT UNIT

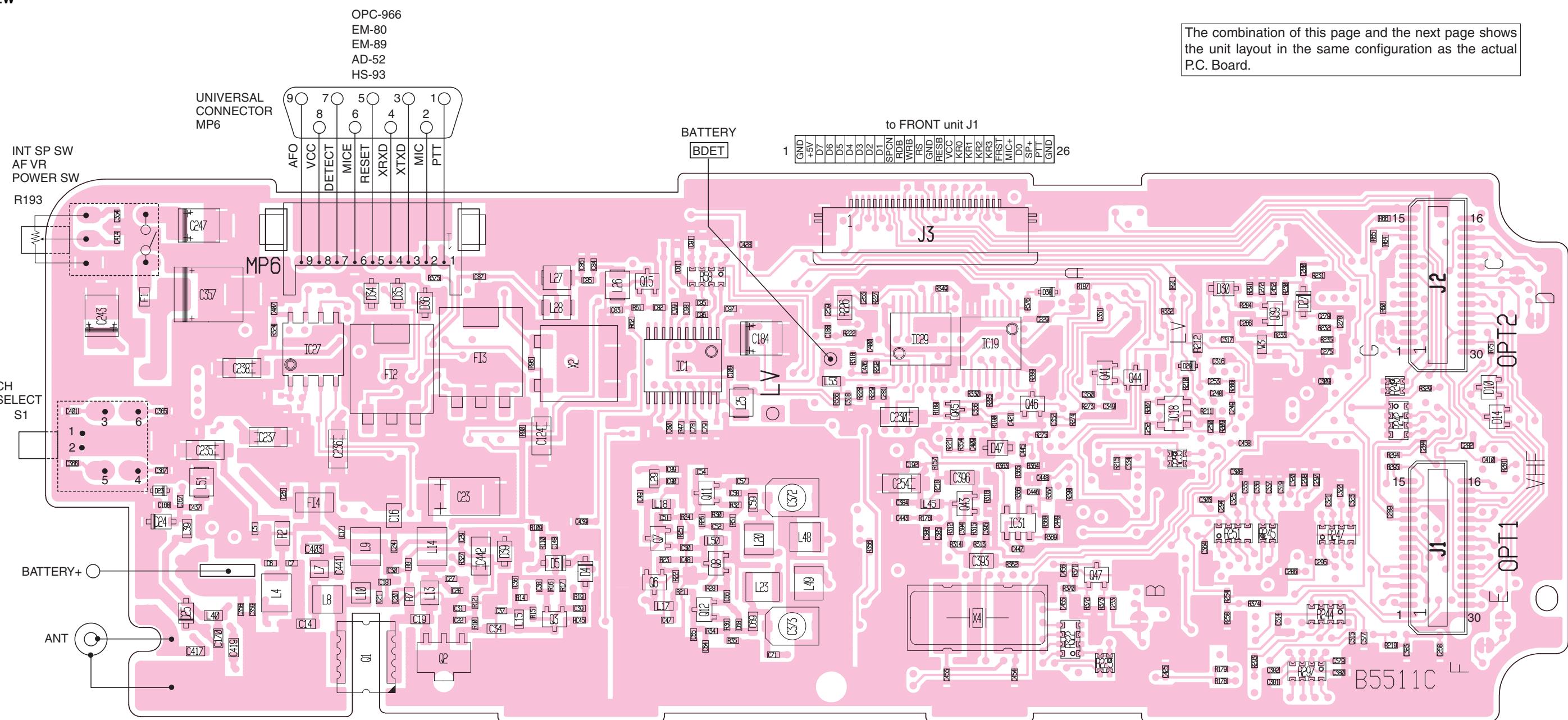
• BOTTOM VIEW

The combination of this page and the previous page shows the unit layout in the same configuration as the actual P.C. Board.



9 - 2 MAIN UNIT

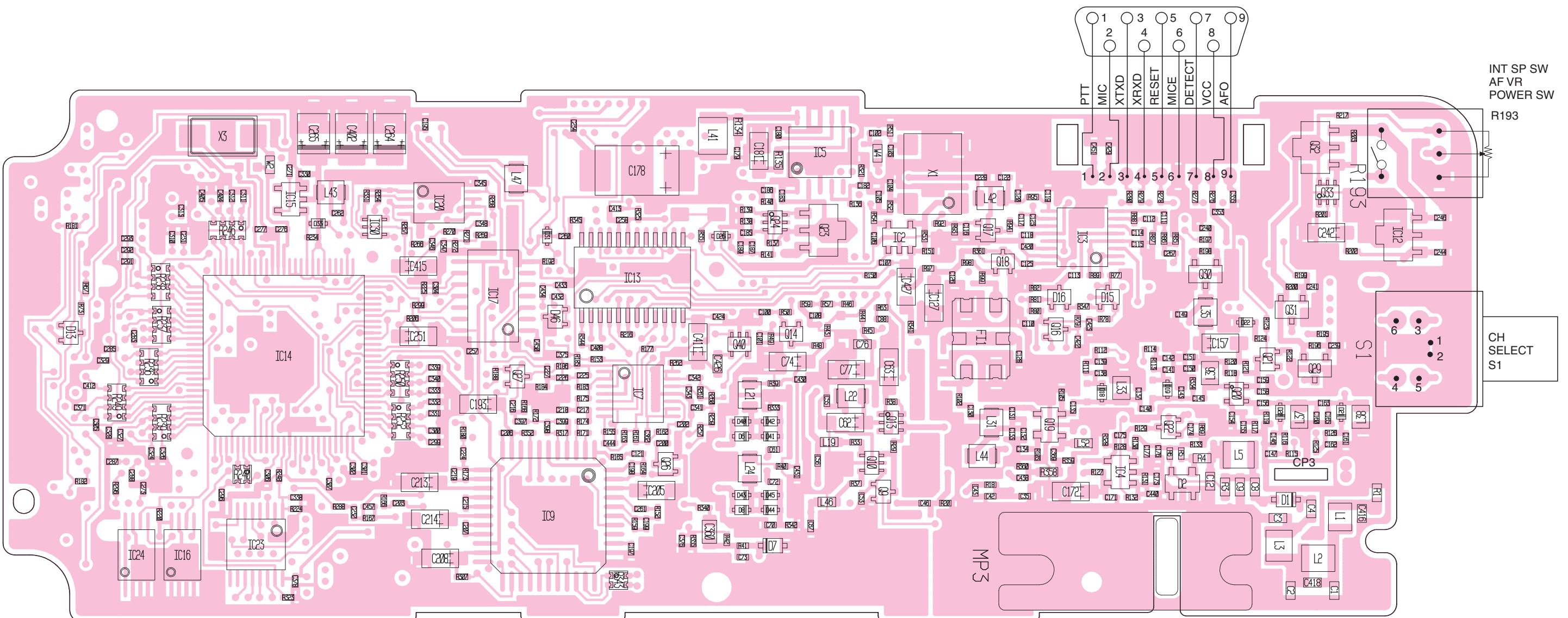
• TOP VIEW



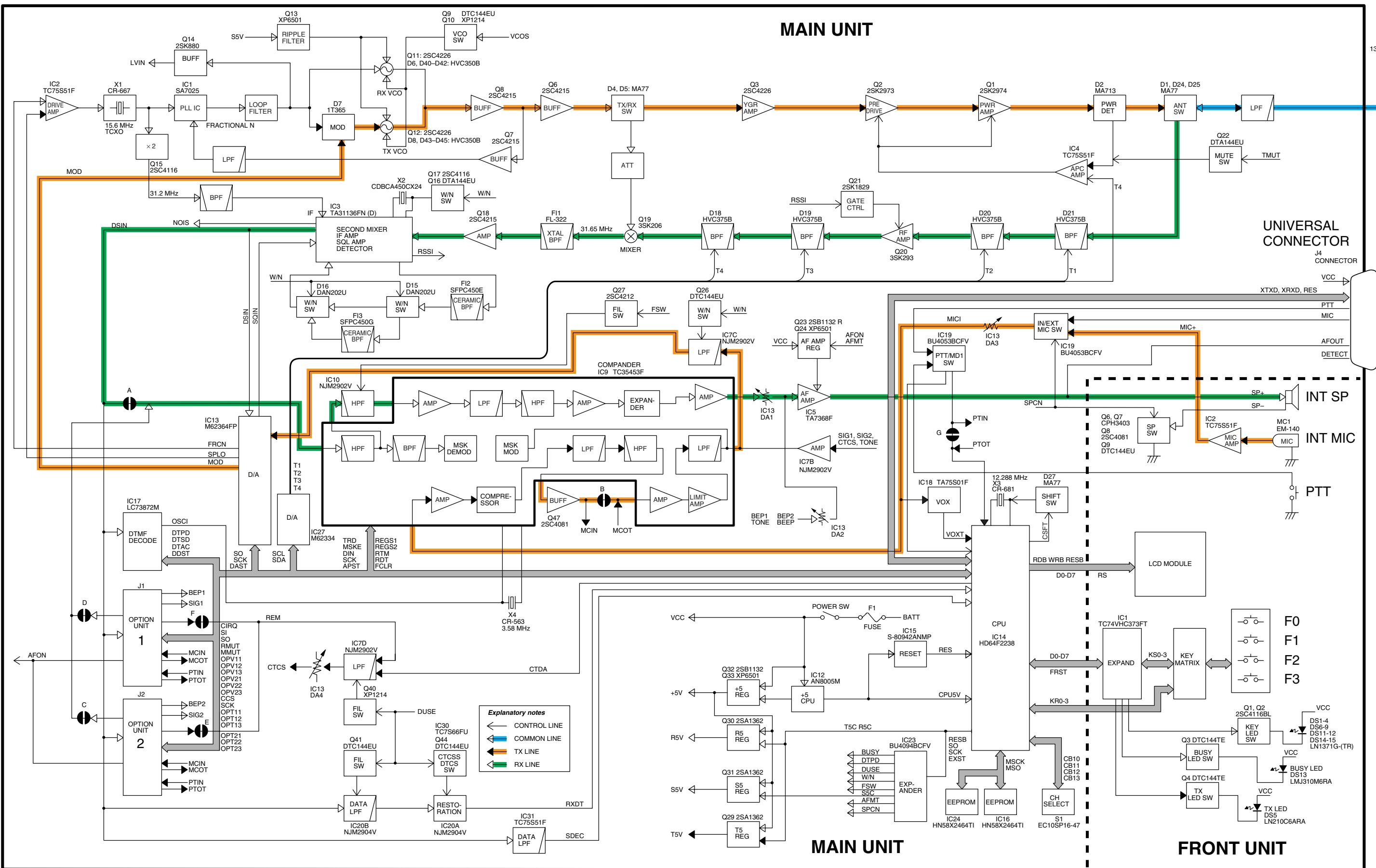
MAIN UNIT

• BOTTOM VIEW

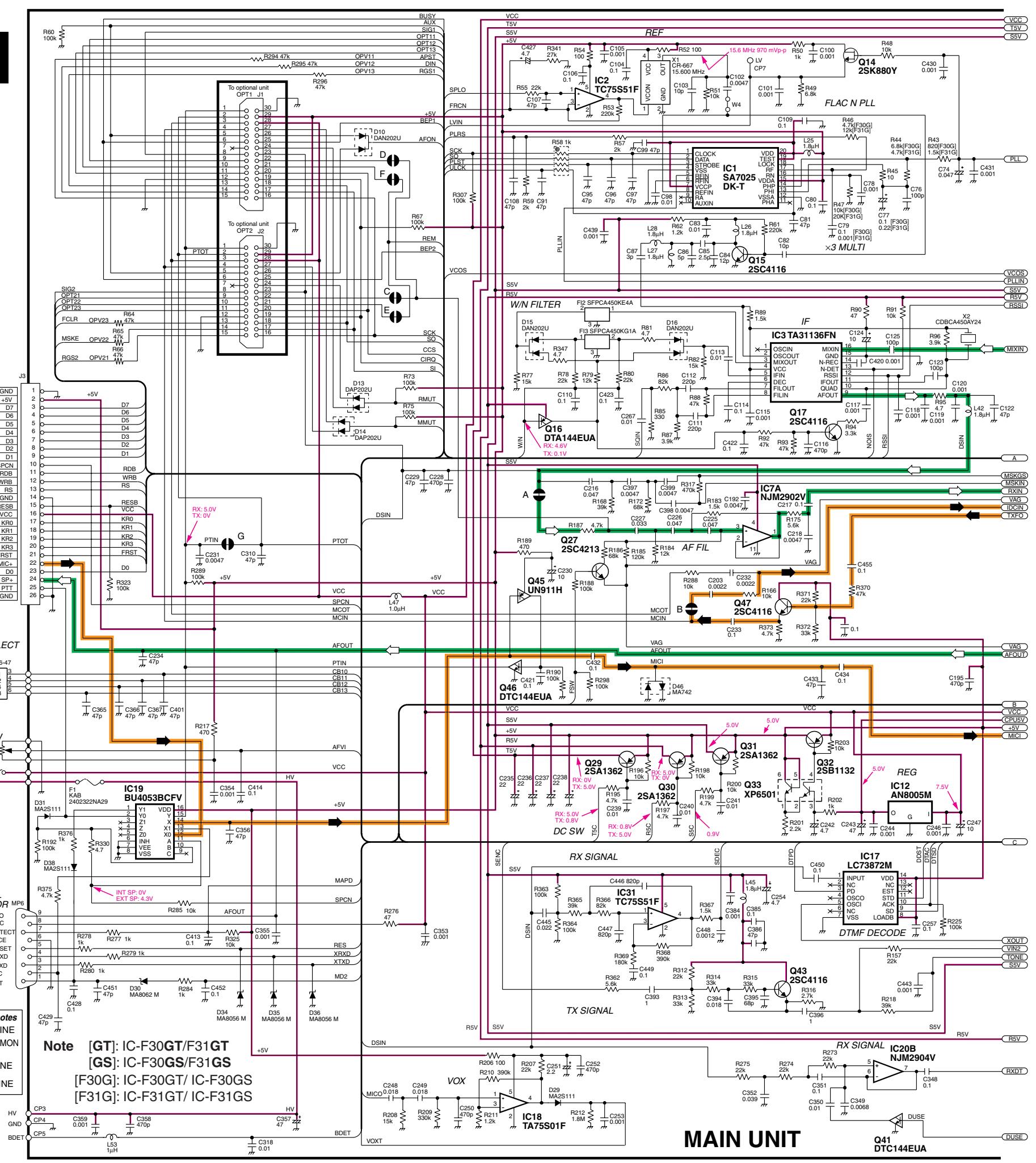
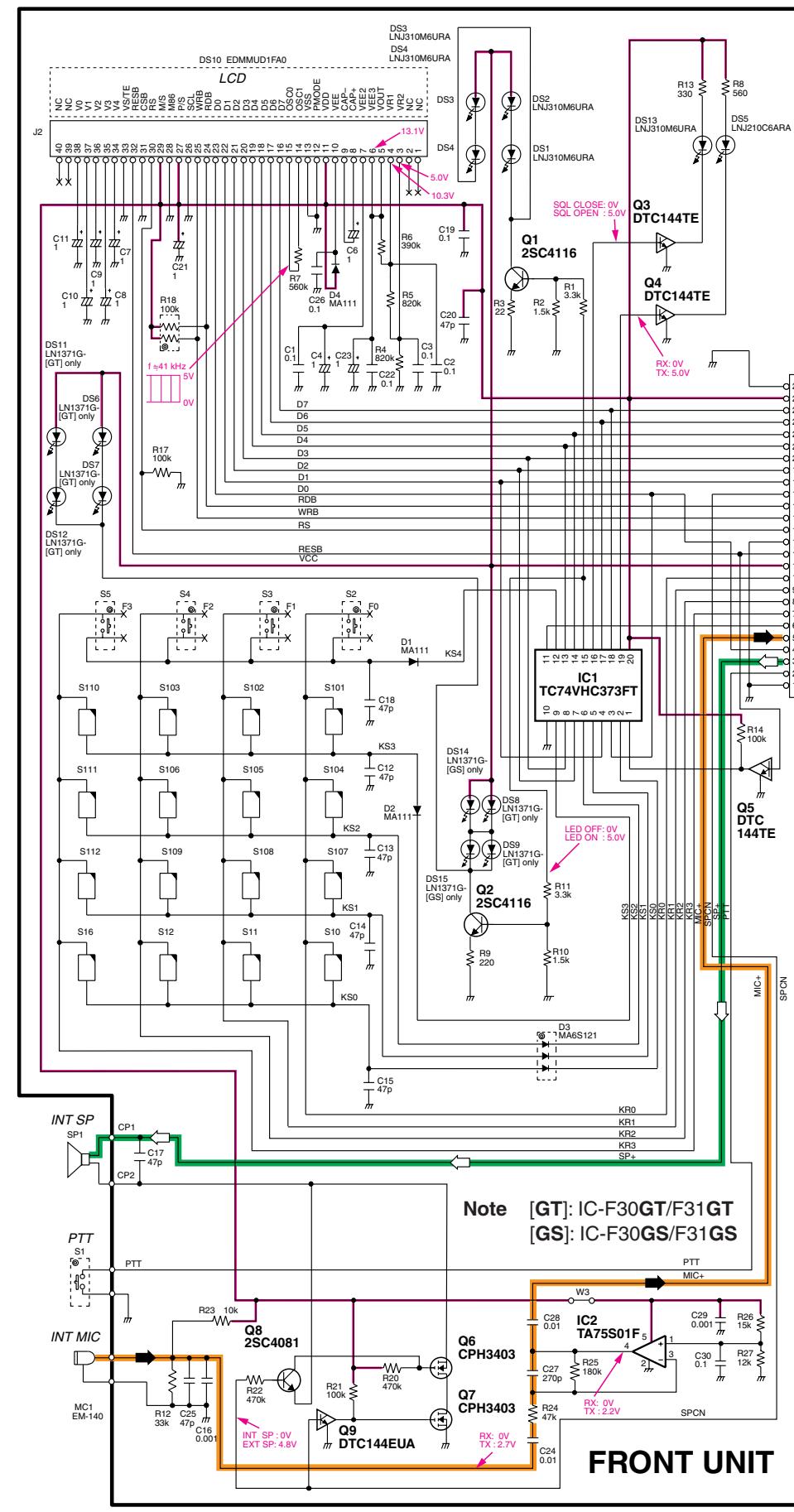
The combination of this page and the previous page shows the unit layout in the same configuration as the actual P.C. Board.

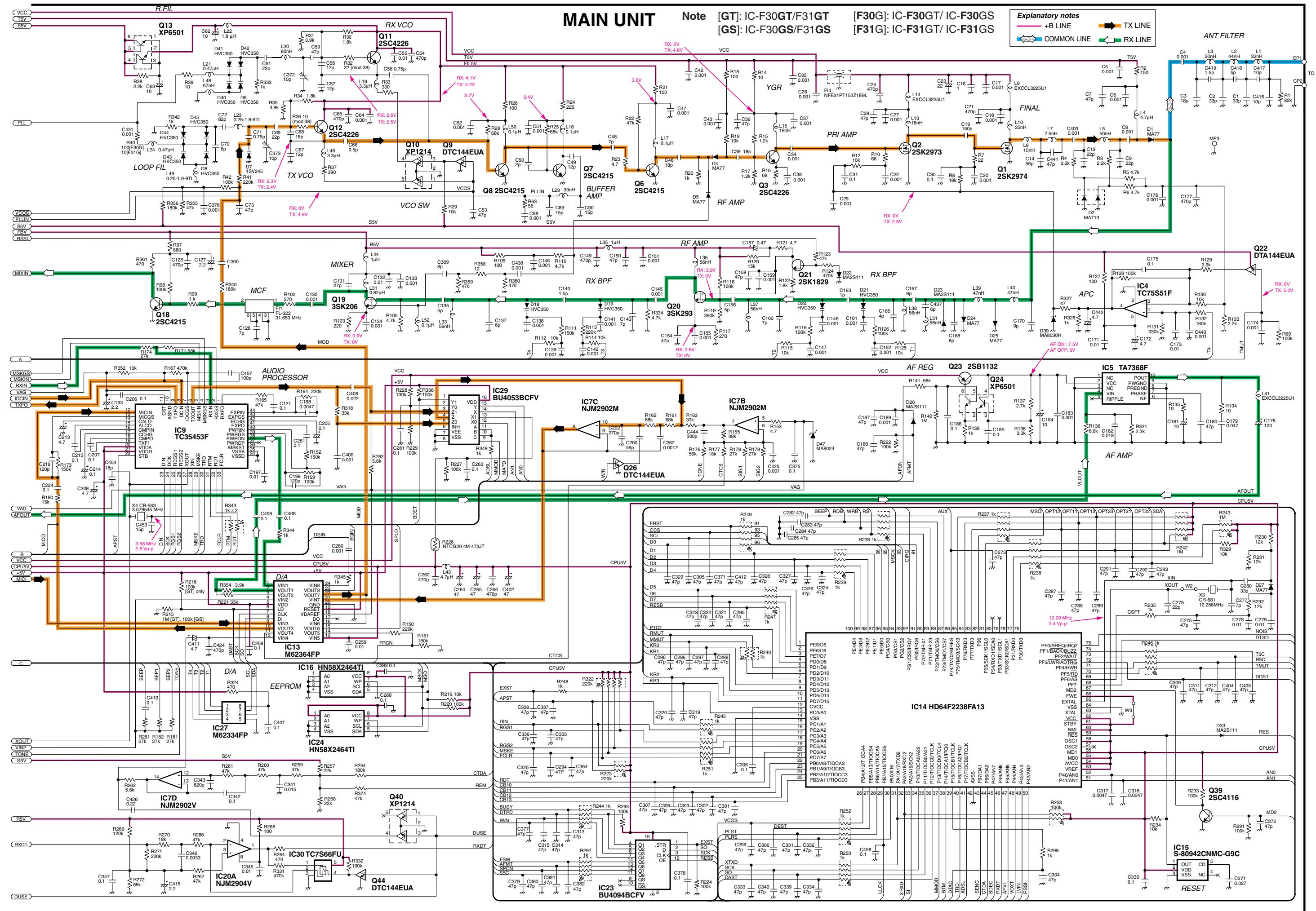


SECTION 10 BLOCK DIAGRAM



SECTION 11 VOLTAGE DIAGRAM





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Count on us!