



SERVICE MANUAL

VHF TRANSCEIVER

IC-F70DT/DS
IC-F70T/S

INTRODUCTION

This service manual describes the latest service information for the **IC-F70DT/DS** and **IC-F70T/S** VHF TRANSCEIVER at the time of publication.

MODEL	10-KEYPAD	APCO25
IC-F70DS	No	Compatible
		Not compatible
IC-F70S	Yes	FM only
		Compatible
IC-F70DT	Yes	Not compatible
		FM only
IC-F70T		

To upgrade quality, any electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

DANGER

NEVER connect the transceiver to an AC outlet or to a DC power supply that uses more than 7.2 V. This will ruin the transceiver.

DO NOT reverse the polarities of the power supply when connecting the transceiver.

DO NOT apply an RF signal of more than 20 dBm (100 mW) to the antenna connector. This could damage the transceiver's front end.

ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

1130010100 S.IC LMX2352TM IC-F70DS MAIN UNIT 5 pieces
8810010120 Screw PH B0 M2×8 SUS ZK IC-F70DS CHASSIS 10 pieces

Addresses are provided on the inside back cover for your convenience.



IC-F70DT/T

REPAIR NOTES

1. Make sure a problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated tuning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 50 dB to 60 dB attenuator between the transceiver and a deviation meter or spectrum analyzer when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.

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SECTION 1 SPECIFICATIONS

■ GENERAL

- Frequency coverage : 136–174 MHz
- Type of emission : 11K0F3E (Narrow)
16K0F3E (Wide)
- Number of conventional channels : 256 channels (Max.)
- Antenna impedance : 50 Ω (Nominal)
- Operating temperature range : -22°F to 140°F
- Power supply requirement : Specified Icom's battery pack only
(Operatable voltage; 7.2 V DC negative ground)
- Current drain (At 7.2 V DC ; approx.) :
- Dimensions (Projections not included) : 2 5/16 (W)× 5 31/32 (H)× 1 1/2 (D) in
- Weight (Except antenna, battery pack) : 8 13/16 oz (Approx.)

RECEIVING		TRANSMITTING	
Stand-by	Max.audio	High (5 W)	Low (1 W)
150 mA	450 mA	2.2 A	1.5 A

■ TRANSMITTER

- Output power (At 7.2 V DC) : High; 5 W, Low; 1 W
- Modulation : Variable reactance frequency modulation
- Maximum permissible deviation : ±2.5 kHz (Narrow)
±5.0 kHz (Wide)
- Frequency error : ±2.00 ppm
- Spurious emissions : 70 dB typ.
- Adjacent channel power : 60 dB min. (Narrow)
70 dB min. (Wide)
- Audio harmonic distortion : 3% typ. at 40% deviation
- Limiting character of modulator : 60–100% of max. deviation
- FM hum and noise (Without CCITT filter) : 34 dB min. (40 dB typ. ; Narrow)
40 dB min. (45 dB typ. ; Wide)
- Audio frequency response : +2 dB to -8 dB of 6 dB/octave from 300 Hz to 2550 Hz (Narrow)
+2 dB to -8 dB of 6 dB/octave from 300 Hz to 3000 Hz (Wide)
- Microphone impedance : 2.2 kΩ

■ RECEIVER

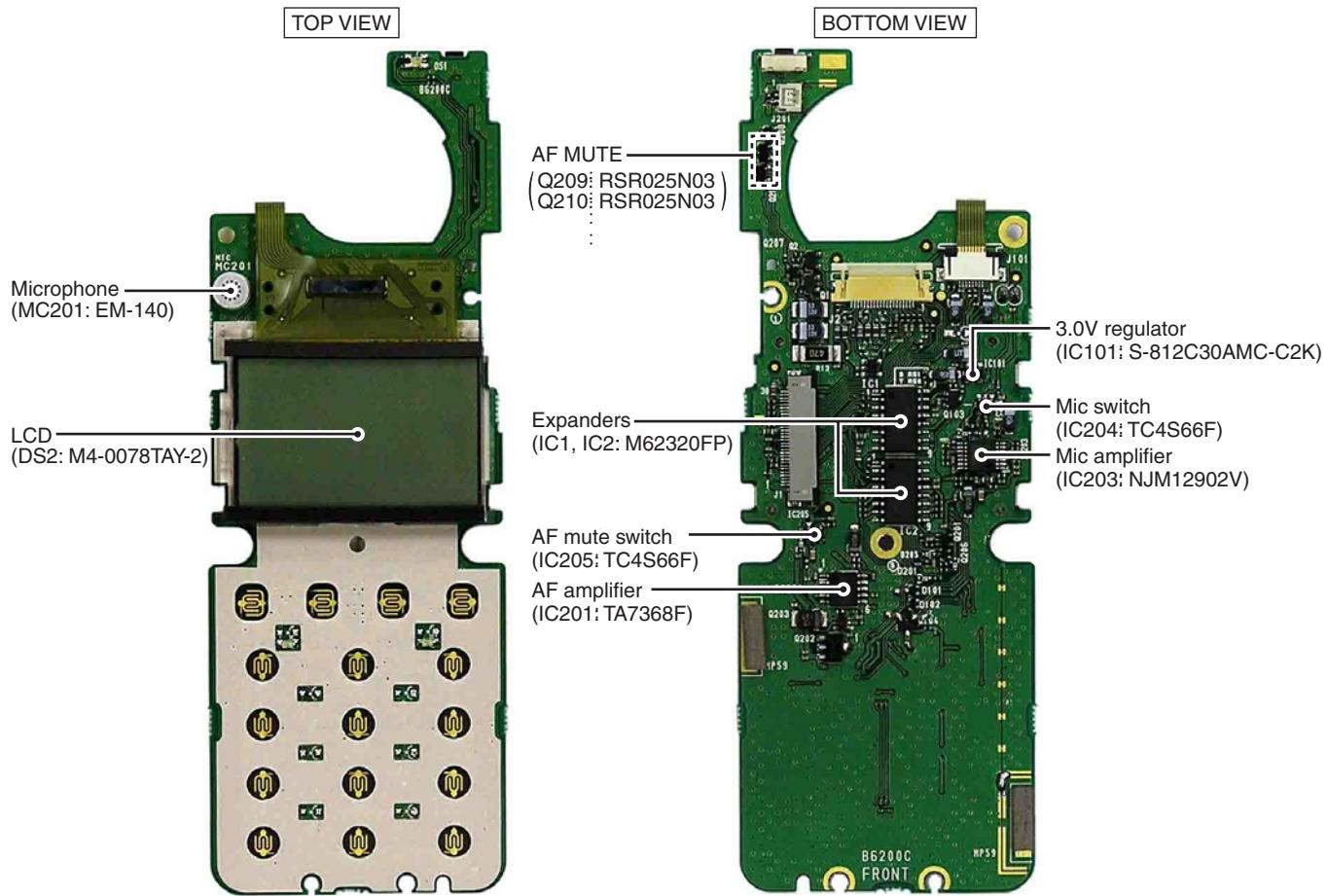
- Receive system : Double conversion superheterodyne system
- Intermediate frequencies : 1st IF; 46.35 MHz, 2nd IF; 450 kHz
- Sensitivity : 0.25 μV typ. at 12 dB SINAD
- Squelch sensitivity (At threshold) : 0.25 μV typ.
- Adjacent channel selectivity : 60 dB min. (70 dB typ. ; Narrow)
70 dB min. (75 dB typ. ; Wide)
- Spurious response : 70 dB min. (80 dB typ.)
- Intermodulation rejection ratio : 70 dB min. (73 dB typ.)
- Hum and Noise (Without CCITT filter) : 34 dB min. (40 dB typ. ; Narrow)
40 dB min. (45 dB typ. ; Wide)
- Audio output power : 0.5 W typ. at 10% distortion with an 8 Ω load
- Output impedance (Audio) : 8 Ω

Specifications are measured in accordance with EIA-152-C/204D, TIA-603

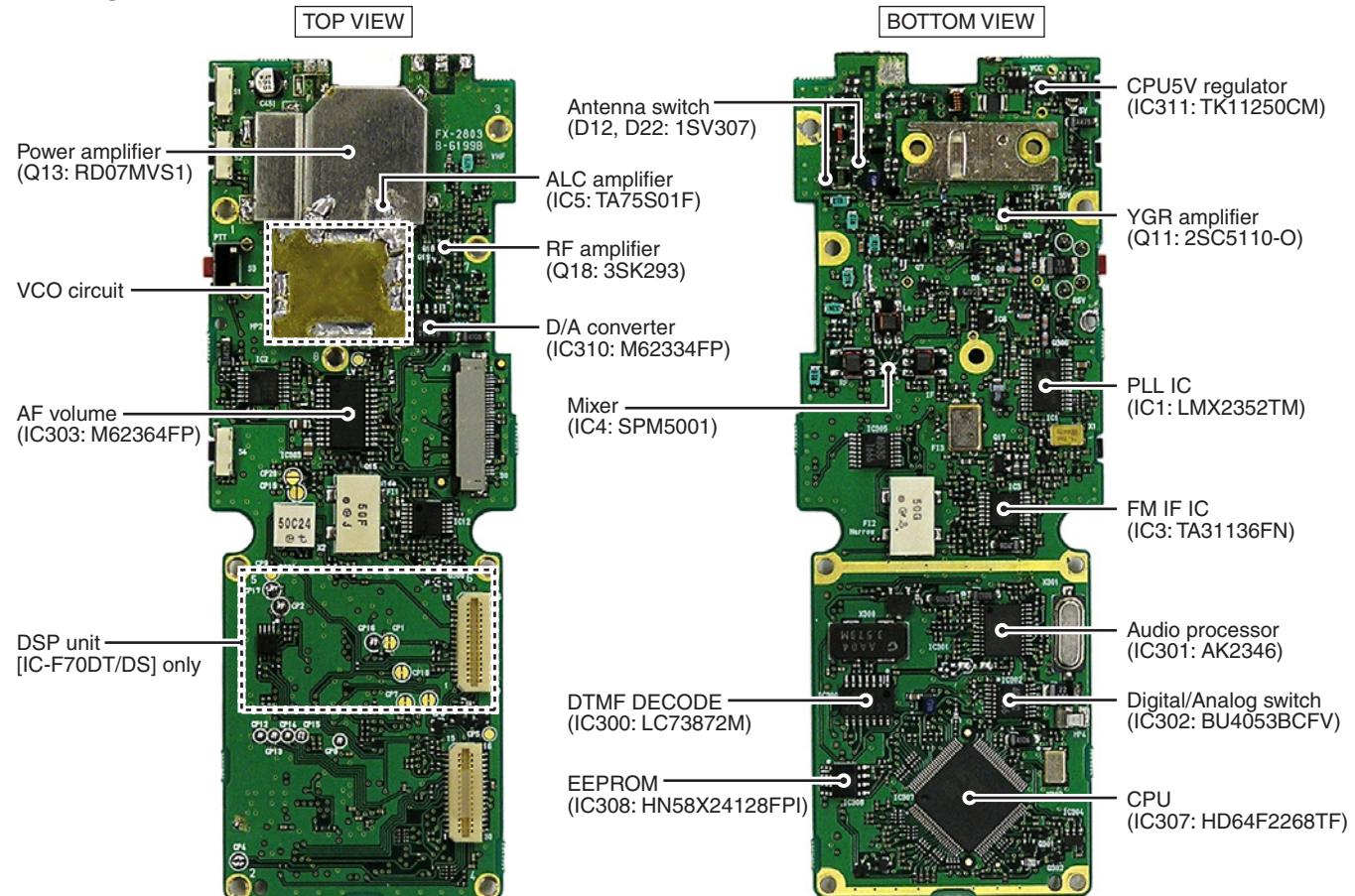
All stated specifications are subject to change without notice or obligation.

SECTION 2 INSIDE VIEWS

• FRONT UNIT



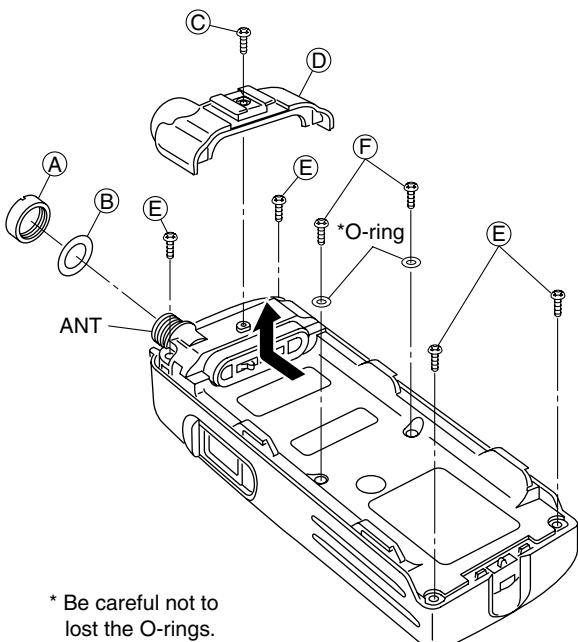
• MAIN UNIT



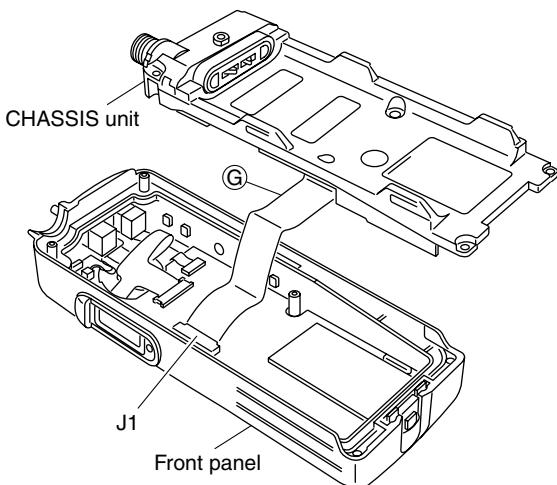
SECTION 3 DISASSEMBLY INSTRUCTIONS

• REMOVING THE CHASSIS UNIT

- ① Unscrew the ANT nut **A** and remove the ANT washer **B**.
- ② Unscrew the screw **C**, and remove the rear panel **D** in the direction of the arrow.
- ③ Unscrew 4 screws **E** and 2 screws **F**.

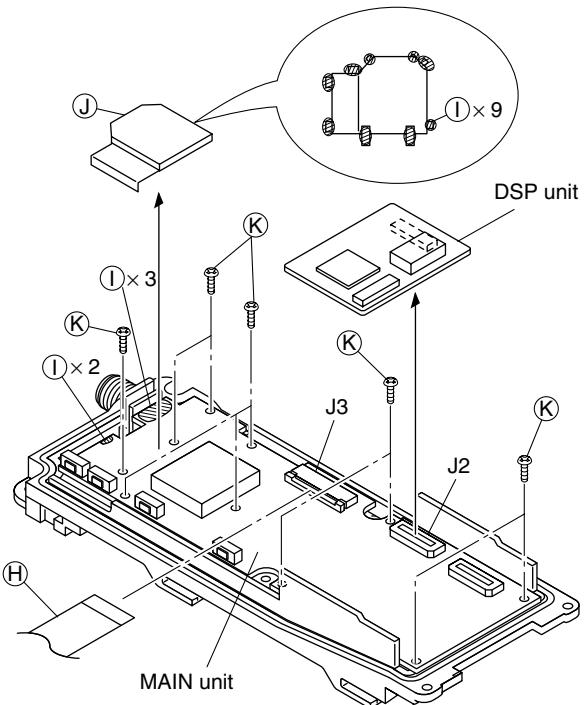


- ⑤ Disconnect the cable **G** from J1 and remove the CHASSIS unit from the front panel.



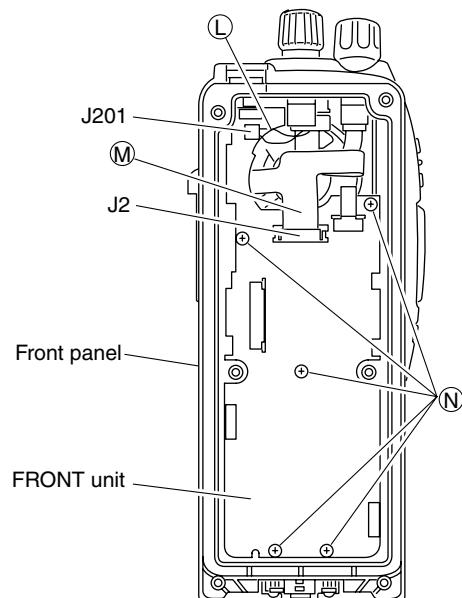
• REMOVING THE MAIN UNIT

- ① Disconnect the cable **H** from J3.
- ② Remove the DSP unit from J2.
- ③ Unsolder 14 points **I** and remove the shield plate **J**.
- ④ Unscrew 10 screws **K** and remove the MAIN unit from the CHASSIS.



• REMOVING THE FRONT UNIT

- ① Disconnect the speaker cable **L** from J201.
- ② Disconnect the cable **M** from J2.
- ③ Unscrew 5 screws **N** and remove the FRONT unit from the front panel.



SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT

The antenna switching circuit toggles the receive line and the transmit line. This circuit does not allow transmit signals to enter the receiver circuits.

Received signals from the antenna connector (CHASSIS UNIT; J1) are passed through a two-stage low-pass filter (LPF; L22, L23, C204–C207, C209) and applied to the $\lambda/4$ type antenna switching circuit (D12, D22).

While receiving, no voltage is applied to D12 and D22. Thus, the receive line and the ground are disconnected and L41, L42, C199–C202 function as a two-stage LPF which leads received signals to the RF circuits via the limiter (D20, D21).

4-1-2 RF CIRCUITS

The RF circuits amplify received signals within the range of frequency coverage and filters off out-of-band signals.

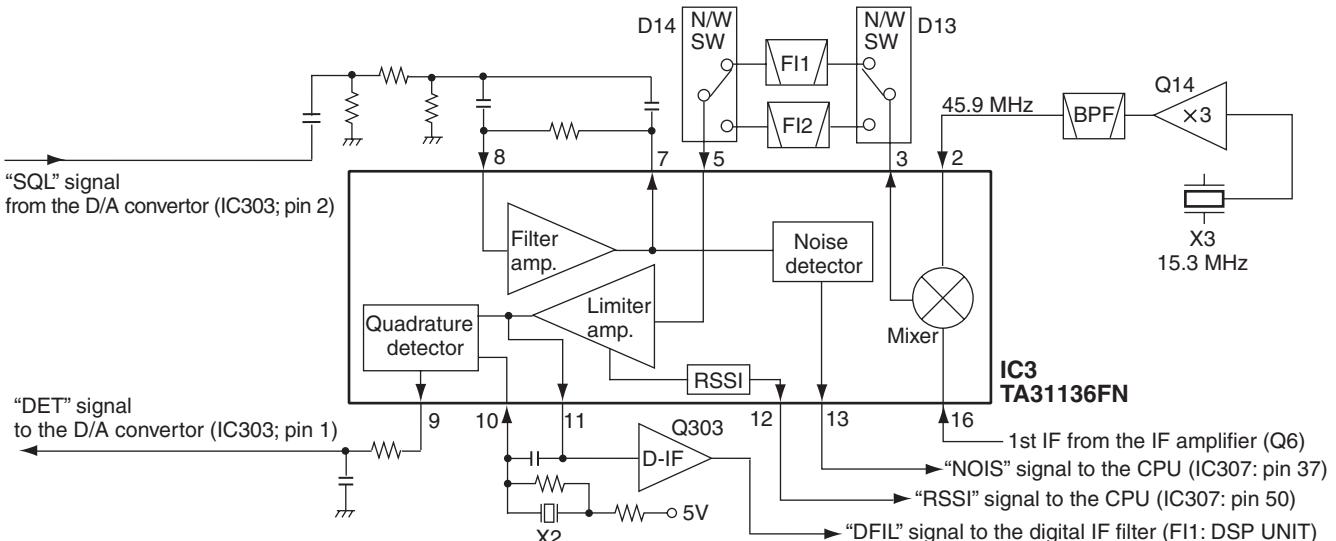
The signals from the antenna switching circuit are passed through the two-stage tunable bandpass filters (BPF; D18, D19, L38, L39, C191, C193, C194, C197, C232, C233) to suppress unwanted signals. The filtered signals are amplified at the RF amplifier (Q18).

The amplified signals are passed through another two-stage tunable BPF (D15, D16, L49, L52–L55, C171, C173, C174, C176) to suppress unwanted signals again. The filtered signals are then applied to the 1st IF circuit.

4-1-3 1st IF CIRCUITS

The 1st mixer circuit converts the received signals into fixed frequency of the 1st intermediate frequency (IF) signal by mixing with the local oscillator (LO) signals which controlled by the PLL circuit. The IF is shifted by changing LO frequency to track the receive signal. The converted 1st IF signal is filtered at the 1st IF filter, then amplified at the 1st IF amplifier.

• 2ND IF AND DEMODULATOR CIRCUITS



The signals from the two-stage tunable BPF are converted into the 46.35 MHz 1st IF signal at the double-balanced type 1st mixer (IC14, L30, L31, L33) by being mixed with the 1st LO signal generated at the RX VCOs (Q4, D4, D5, D24, D26 or Q20, D27 to D30).

The 1st IF signal from the 1st mixer is passed through the crystal filter (FI3) to suppress unwanted signals, and then amplified at the 1st IF amplifier (Q17). The amplified 1st IF signal is applied to the FM IF IC (IC3, pin 16).

4-1-4 2nd IF AND FM DEMODULATOR CIRCUITS

The 1st IF signal is converted into the 2nd IF signal and demodulated at the detector section in the FM IF IC. The FM IF IC contains 2nd mixer, limiter amplifier, quadrature detector, etc. in its package.

The 1st IF signal from the 1st IF amplifier (Q17) is applied to the mixer section in FM IF IC (IC3, pin 16). The applied 1st IF signal is mixed with the 45.9 MHz 2nd LO signal generated by tripling the 15.3 MHz PLL reference frequency to be converted into the 450 kHz 2nd IF signal.

The 2nd IF signal from the mixer section is output from pin 3 and passed through the N/W switches (D13, D14) and ceramic filter (FI1 or FI2) to suppress the heterodyne noise.

The N/W switches (D13, D14) toggle the receive mode wide and narrow according to "NWC" signal from the CPU (IC307, pin 19). FI1 is used for wide, and FI2 is used for narrow mode operation.

The filtered signal is applied to IC3 (pin 5) again, and amplified at the limiter amplifier section and demodulated by the quadrature detector.

The quadrature detector is a detection method which uses a ceramic discriminator (X2).

The demodulated AF signals are output from pin 9, and applied to the AF circuits.

4-1-5 AF CIRCUITS

The demodulated AF signals from the FM IF IC are amplified and filtered at AF circuit. This transceiver employs the base band IC for audio signal processing for both transmit and receive. The base band IC is an audio processor and composed of pre-amplifier, compressor, expander, scrambler, etc. in its package.

The AF signals from FM IF IC (IC3, pin 9) are applied to the base band IC (IC301, pin 23) via the digital/analog switch (IC302, pins 12, 14).

The applied AF signals are amplified at the amplifier section and level adjusted at the volume control section, and then suppressed unwanted 3 kHz and higher audio signals at LPF section. The filtered AF signals are applied or bypassed the TX/RX HPF, scrambler, de-emphasis, sections in sequence, then applied to another volume controller.

The TX/RX HPF filters out 250 Hz and lower audio signals, and the de-emphasis obtains -6 dB/oct of audio characteristics. The expander expands the compressed audio signals and also noise reduction function is provided.

The AF signals are level adjusted at the volume controller and amplified at the amplifier section. The amplified AF signals are output from pin 20 and applied to the D/A converter (IC303, pin 16) to be adjusted its level, and then applied to the FRONT UNIT via J3 (pin 28).

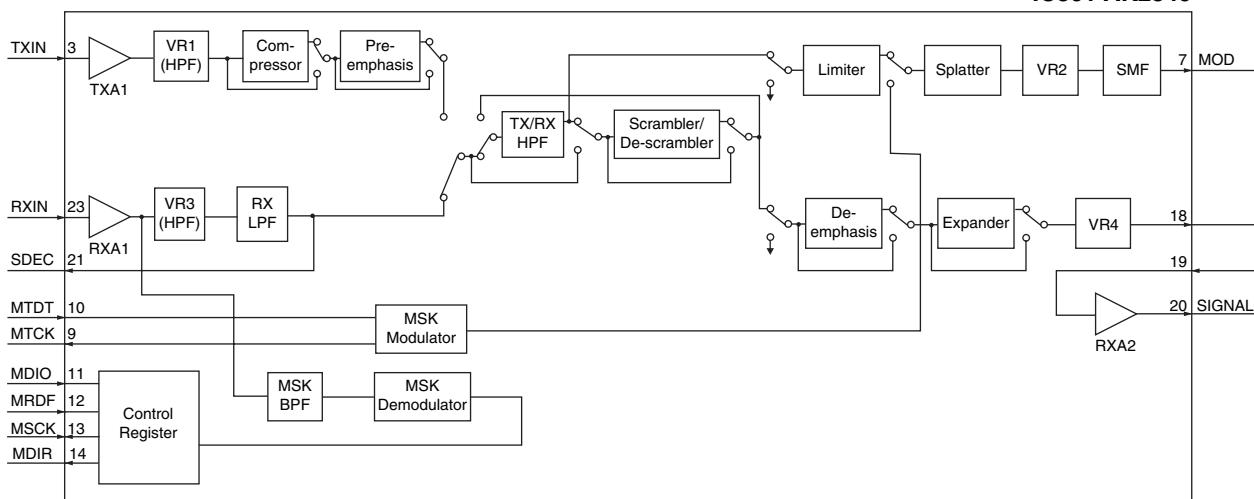
The level controlled AF signals from the MAIN UNIT are passed through the mute switch (FRONT UNIT; IC205, pins 1, 3) and applied to the AF power amplifier (IC201, pin 4: FRONT UNIT) to obtain 500 mW of AF output power. The power amplified AF signals are applied to the internal speaker (CHASSIS UNIT; SP1).

4-1-6 SQUELCH CIRCUITS

• NOISE SQUELCH

Noise squelch circuit mutes AF output signals when no RF signals are received. By detecting noise components in the

• BASE BAND IC BLOCK DIAGRAM



demodulated AF signals, the squelch circuit switches the AF mute switch and AF power amplifier controller ON and OFF.

A portion of the demodulated AF signals from the FM IF IC (IC3, pin 9) are applied to the converter (IC303, pin 1) to be adjusted its level. The level controlled signals are output from pin 2 and applied to the active filter (IC3, pins 7, 8; R74, R75, R77 C137–C139). The filtered signals are applied to the filter amplifier section to amplify the noise components only.

The amplified noise components are converted into the pulse-type signal at the noise detector section, and output from pin 13 as the "NOIS" signal and applied to the CPU (IC307, pin 37). Then the CPU outputs "AFON" signal from pin 18 according to the "NOIS" signal level to toggle the AF mute circuit (FRONT UNIT; IC205) and AF amplifier controller (FRONT UNIT; Q202, Q203) ON/OFF.

• CTCSS AND DTCS

The tone squelch circuit detects tone signals and opens the squelch only when receiving a signal containing a matched sub audible tone (CTCSS or DTCS). When the tone squelch is in use, and a signal with a mismatched or no sub audible tone is received, the tone squelch circuit mutes the AF signals even when the noise squelch is open.

A portion of the demodulated AF signals are passed through the LPF (IC12, pins 12, 14) to filters CTCSS/DTCS signal. The filtered signal is applied to the CPU (IC307, pin 46) after being amplified at the buffer amplifier (IC2, pins 1, 3).

The CPU compares the applied signal and the set CTCSS/DTCS, then output the AF mute switch (IC205) AF amplifier controller (Q202, Q203) control signal from pin 18.

4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT

The microphone amplifier circuit amplifies the audio signals from microphone within +6 dB/oct pre-emphasis characteristic. The microphone signals are processed in the base band IC which contains microphone amplifier, compressor, scrambler, limiter, splatter filter, etc. in its package.

The audio signals from the microphone (FRONT UNIT; MC201) are passed through the microphone mute switch (FRONT UNIT; IC204). The switched signals are amplified at the microphone amplifiers (FRONT UNIT; IC203, pins 1, 2, 13, 14) to obtain within +6 dB/oct pre-emphasis characteristics. The amplified signals are applied to the MAIN UNIT via J1 (pin 2).

The amplified MIC signals from the FRONT UNIT are applied to the base band IC (IC301, pin 3). The applied MIC signals are amplified at the amplifier section, and level adjusted at the volume control section. The level adjusted MIC signals are applied or bypassed the compressor section, pre-emphasis section, TX/RX HPF, de-scrambler, limiter, splatter, in sequence, then applied to another volume controller.

The compressor compresses the MIC signals to provide high S/N ratio for receive side, and the pre-emphasis obtains +6 dB/oct audio characteristics. The TX/RX HPF filters out 250 Hz and lower audio signals, the limiter limits its level and the splatter filters out 3 kHz and higher audio signals.

The filtered MIC signals are level adjusted at another volume control section and amplified at the amplifier section, and then output from pin 7 via smoothing section (SMF).

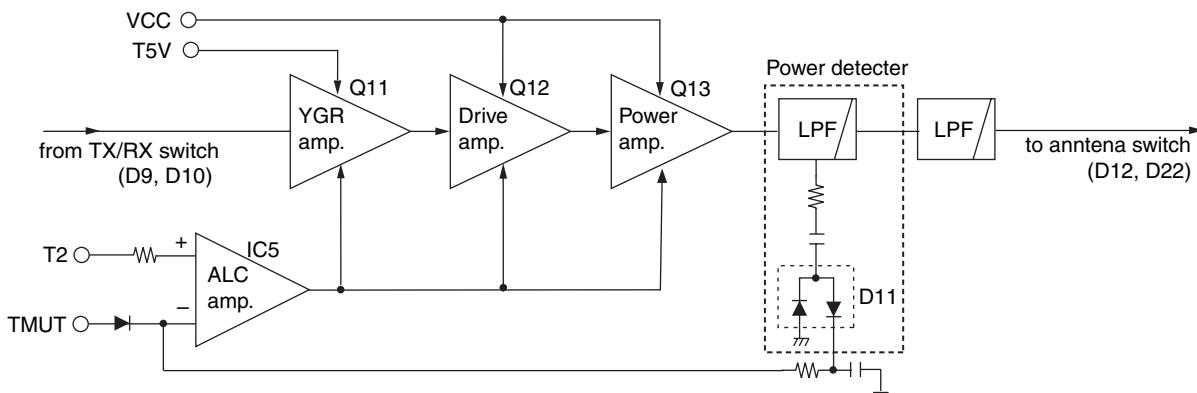
4-2-2 MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal with the audio signals from the microphone.

MIC signals from the base band IC (IC301) are passed through the MIC switch (IC302, pins 5, 4), PM filter (C338, R327), FM/PM switch (IC302, pins 1, 15), and then applied to the AF mixer (IC12, pin 2) to be mixed with CTCSS/DTCS signals.

The mixed MIC signals are applied to the D/A converter (IC303, pin 4) to be adjusted its level. The level adjusted AF signals are output from pin 3 and applied to the modulation circuit (D8) to modulate the VCO oscillating signal by changing the reactance of D8 at the TX VCO (Q5, D6, D7, D25).

• ALC CIRCUIT



The CTCSS/DTCS signals are generated by the CPU (IC307) and output from pins 89–91 ("CENC0," "CENC1," "CENC2"). The CTCSS/DTCS signals are passed through 3 registers (R374–R376) to change its wave form. The wave form changed CTCSS/DTCS signals are then passed through the LPF (IC12, pins 8, 10) and applied to the converter (IC303, pin 9) to be adjusted its level, and output from pin 10.

The level adjusted CTCSS/DTCS signals are applied to the AF mixer (IC12, pin 2) to be mixed with MIC signals. The mixed CTCSS/DTCS signals are output from pin 1 and applied to the D/A converter (IC303, pin 4) to be adjusted its level again, then output from pin 3. The CTCSS/DTCS signals from the D/A converter are applied to the both of reference frequency oscillator (X1) and modulation circuit (D8) to modulate the reference frequency signal and VCO oscillating signal.

The modulated VCO output signal is amplified at the buffer amplifiers (Q6, Q10) and is then applied to the YGR amplifier (Q11) via the TX/RX switch (D10).

4-2-3 TRANSMIT AMPLIFIERS

The VCO output signal is amplified to transmit output power level by the transmit amplifiers .

The buffer-amplified signal from the TX/RX switch is applied to the YGR (Q11), the driver (Q12), and power (Q13) amplifiers, to be amplified to the transmit output power level. The power amplified transmit signal is passed through the power detector (D11), antenna switch (D12), and two-stage LPFs (L22, L23, C204–C207, C209), and then applied to the antenna connector (CHASSIS UNIT; J1).

4-2-4 ALC CIRCUIT

The ALC (Automatic Level Control) circuit stabilizes transmit output power and controls transmit output power High or Low.

The power detector circuit (D11) detects the transmit output signal and converts it into DC voltage.

The detected voltage is applied to the ALC amplifier (IC5, pin 3). The "T2" signal from the D/A converter (IC310, pin 2), controlled by the CPU (IC307), is applied to the another input (pin 1) for reference, and the "T2" signal also controls transmit output power (5 W or 1 W).

The output voltage from the ALC amplifier controls the bias of the YGR (Q11), driver (Q12) and power amplifier (Q13) to reduce the output power by comparing the detected voltage and the reference voltage. Thus the ALC circuit maintains a constant transmit output power.

4-3 PLL CIRCUITS

4-3-1 PLL CIRCUIT (MAIN UNIT)

The PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL circuit compares the phase of the divided VCO frequency with the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of the programmable divider.

The PLL circuit contains the two RX VCOs (Q4, D4, D5, D24, D26 for 154–174 MHz, Q20, D27–D30 for 136–153.995 MHz) and one TX VCO (Q5, D6, D7, D25). The oscillated signal is amplified at the buffer amplifiers (Q6, Q9) and applied to the PLL IC (IC1, pin 6) after being passed through the BPF (Q1, D1, D2, L2, L56, L57, L302, C12, C15, C20, C22, C25–C28, C32).

Q1, D1 and D2 compose of a BPF switch which toggles the filtering frequencies for TX and RX, controlled by "T5C" signal from the CPU (IC307 pin 16).

The applied signal is divided at the prescaler and programmable divider section by the N-data ratio from the CPU. The divided signal is detected at the phase detector section via divided ratio adjustment section using the reference frequency passed through the reference divider and output from pin 4 after being passed through the charge pump section. The output signal is passed through the loop filter (R16, R17, C17, C24, C29, C31) and is then applied to the VCO circuits.

If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

4-3-2 VCO CIRCUITS

The VCO circuits contain separate two RX VCOs (Q4, D4, D5, D24, D26 for 154–174 MHz, Q20, D27–D30 for 136–153.995 MHz) and one TX VCO (Q5, D6, D7, D25). The oscillated signal is amplified at the buffer amplifiers (Q6, Q10) and is then applied to the TX/RX switch (D9, D10). Then the receive 1st LO (RX) signal is applied to the 1st mixer (IC14, L30, L31, L33), and the transmit (TX) signal is applied to the YGR amplifier (Q11).

A portion of the signal from the buffer amplifier (Q6) is fed back to the PLL IC (IC1, pin 6) via the buffer amplifier (Q9) and the BPF (Q1, D1, D2, L2, L56, L57, L302, C12, C15, C20, C22, C25 to C28, C32) as the comparison signal.

4-4 POWER SUPPLY CIRCUITS

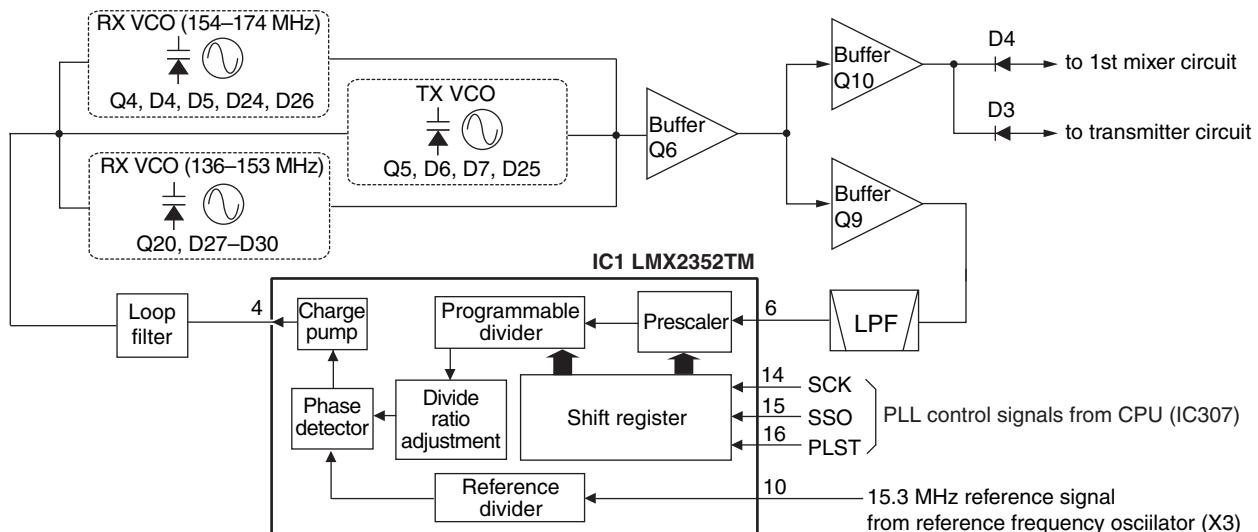
4-4-1 VOLTAGE LINES (MAIN UNIT)

LINE	DESCRIPTION
VCC	The voltage from the attached battery pack passed through the power switch (Q309).
CPU5V	Common 5 V for the CPU (IC307) converted from the VCC line at the CPU5V regulator (IC311).
+5V	Common 5 V line converted from the VCC line at the +5V regulator (Q307, Q308).
T5V	5 V for the transmit circuits regulated from the +5V line by the T5V switch (Q305). The switch is controlled by the "T5C" signal from the CPU (IC307, pin 16).
S5V	5 V for the power save line regulated from the +5V line by the S5V switch (Q304). The switch is controlled by the "S5C" signal from the CPU (IC307, pin 27).
R5V	5 V for the receive circuits regulated from the +5V line by the R5V switch (Q306). The regulator is controlled by the "R5C" signal from the CPU (IC307, pin 26).

4-4-2 VOLTAGE LINES (DSP UNIT)

LINE	DESCRIPTION
DVDD3.3V	3.3 V for the CPU (IC12; DSP UNIT), DSP IC (IC7) and EEPROM (IC17) regulated from the +5V line by the +3VC regulator (IC1).
CVDD1.5V	1.5 V for the DSP IC (IC7) converted from the +5V line at the +1.5VA regulator (IC2).
+3VD	3.3 V for the A/D converter (IC8) and LINER CODEC IC (IC9) from the +5V line at the +3VD regulator (IC3).

• PLL CIRCUIT



4-5 DIGITAL CIRCUIT (IC-F70DT/DS only)

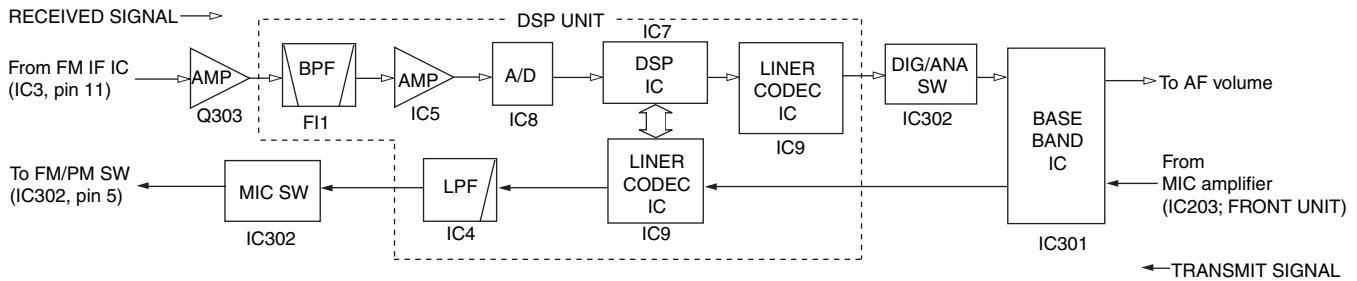
• WHILE RECEIVING

A portion of the 2nd IF signal from the limiter amplifier section in the FM IF IC (IC3) is output from pin 11 and is applied to the 2nd IF amplifier (Q303). The amplified 2nd IF signal is applied to the DSP UNIT via J2 (pin 11).

The 2nd IF signal from the MAIN UNIT is passed through the ceramic BPF (DSP UNIT; FI1) to suppress heterodyne noise, and amplified again at the digital IF amplifier (DSP UNIT; IC5, pin 4). The amplified 2nd IF signal is applied to the A/D converter (DSP UNIT; IC8, pin 3) to be converted into digital IF data, then applied to the DSP IC (DSP UNIT; IC7). The DSP IC converts the digital IF into the digital audio signal.

The digital audio signal from the DSP IC are converted into analog audio signals at the LINER CODEC IC (IC9) and output from pin 16. The audio signals from the LINER CODEC IC are applied to the MAIN UNIT via J1 (pin 22).

• DIGITAL MODE BLOCK DIAGRAM



4-6 PORT ALLOCATIONS

4-6-1 CPU (IC307)

Pin number	Port name	Description
4–7	R1, R2, R4, R8	Input ports for rotary selector (VR UNIT; S1).
10	SSO	Outputs serial data to the PLL IC (IC1, pin 15) and D/A converter (IC303, pin 8).
11	SCK	Outputs clock signal to the PLL IC (IC1 pin 14) and D/A converter (IC303, pin 7), etc.
13	PLST	Outputs strobe signals to the PLL IC (IC1, pin 16).
15	DASW	Outputs control signal to the digital/analog switch (IC302). Low: While analog mode is selected.
16	TXC	Outputs the T5V switch (Q305) control signal. Low: During transmit.
17	TMUT	Outputs the ALC amplifier (IC5) control signal. Low: During receive.
18	AFON	Outputs control signal for AF mute circuit (FRONT UNIT; IC205) and AF power amplifier (FRONT UNIT; IC201). High: AF amplifier (IC201) is activated.
19	NWC	Outputs wide/narrow switch (D13, D14) control signal. High: When narrow mode is selected.

The audio signals from the DSP UNIT are applied to the base band IC (MAIN UNIT; IC301, pin 20) after being passed through the digital/analog switch (MAIN UNIT; IC302).

• WHILE TRANSMITTING

The microphone signals from the base band IC (IC301, pin 7) are applied to the DSP UNIT via J2 (pin 4).

The microphone signals from the MAIN UNIT are applied to the LINER CODEC IC (DSP UNIT; IC9, pin 2) to convert into the digital audio signal.

The converted digital audio signal is processed by the DSP IC (DSP UNIT; IC7), and applied to the LINER CODEC IC (DSP UNIT; IC9) again. The signal from the LINER CODEC IC (IC9, pin 15) is passed through the LPFs (DSP UNIT; IC4, pins 3, 4, 5, 7) and applied to the MAIN UNIT via J1, and then passed through the microphone switch (MAIN UNIT; IC302, pins 3, 4), FM filter (R328, C335), FM/PM switch (IC302, pins 2, 15).

Pin number	Port name	Description
20	DDSD	Input port for serial data from the DTMF decoder IC (IC300, pin 9).
21	DDAC	Outputs clock signals to the DTMF decoder IC (IC300, pin 10).
26	R5C	Outputs R5V switch (Q306) control signal. High: While receiving.
27	S5C	Outputs S5V switch (Q304) control signal. High: In power save mode..
29	PTTO	Input port for optional unit. Low: Switch ON.
30	EM	Input port for the emergency switch (FRONT UNIT; S117). Low: While emergency switch is pushed.
32	RMUT	Input port for the AF mute signal from the optional unit via J1 or J2. Low: While RX audio is muted.
33	MMUT	Input port for the microphone mute signal from the optional unit via J1 or J2. Low: While microphone audio is muted.
34–36	OPT1–OPT3	I/O ports for the connected optional unit to J1.

4-6-1 CPU (continued)

Pin number	Port name	Description
37	NOIS	Input port for the noise signal from the FM IF IC (IC3, pin 13).
38	PWRSW	Input port for the [VOL] control (VR UNIT; R1). Low: While power is ON.
39	DDST	Input port for the decodedDTMF signals from the DTMF decoder IC (IC300, pin 11).
40	CIRQ	Inputs offering signal from the optional unit and DSP unit. Low: Offering signal is output.
41	PWRO	Outputs control signal for the power switch circuit (Q309, Q310). High: Power ON.
43	SENC	Outputs single tone encode signal.
44	BEEP	Outputs beep audio signals.
45	SDEC	Input port for single tone decode signal from the base band IC (IC301, pin 1).
46	CDEC	Input port for CTCSS/DTCS signal from the LPF (IC12, pin 7).
47	ULCK	Input port for the PLL unlock signal. Low: The PLL circuit is unlocked.
48	BATV	Input port for the connected battery pack for the low battery voltage detection. Low: The battery voltage is low.
49	LVIN	Input port for the PLL lock voltage.
50	RSSI	Input port for the "RSSI" signal from the FM IF IC (IC3, pin 12).
51	TEMP/OPTV	<ul style="list-style-type: none"> • Input port for the transceiver's internal temperature detecting signal. High: Internal temperature is high. • Input port for the optional unit detecting signal. High: While connecting optional unit to the multiconnector.
55	SIDE1	Input port for [UP] switch (MAIN UNIT; S1). Low: While [UP] switch is pushed.
68	DAST	Outputs strobe signals to the D/A converter (IC303, pin 6).
69	DSDA	I/O port for data signal to the D/A converter (IC310, pin 6).
72	SPCON	Outputs "SPCON" signal. Low: Audio output.
78	MTCK	Input port for transmitting MSK clock signal from the base band IC (IC301, pin 9).
79	KR	Input port for key matrix. Low: While any of key on the 10-keypad (including [P0]–[P3]) is pushed.
80	FSDA	I/O port for the serial data signal for the expander (FRONT UNIT; IC2).
81	FSCL	Outputs clock signal to the expander (FRONT UNIT; IC2).
88	SIDE2	Input port for [DOWN] switch (MAIN UNIT; S2). Low: While [DOWN] switch is pushed.

Pin number	Port name	Description
89–91	CENC0–CENC2	Output the CTCSS/DTCS signals.
92	SIDE3	Input port for [MONITOR] switch (MAIN UNIT; S4). Low: While [MONITOR] switch is pushed.
93	MTDT	Outputs the MSK data to the base band IC (IC301, pin 10).
94	MDIR	Outputs serial data control signal to the base band IC (IC301, pin 14).
95	MDIO	I/O port for the serial data signals from/to the base band IC (IC301, pin 11).
96	MSCK	Outputs clock signal for the base band IC (IC301, pin 13).
97	PMFM	Outputs the FM/PM switch (IC302, pin 11) control signal. High: While PM is selected.
98	ESDA	I/O port for data signals from/to the EEPROM (IC308, pin 5).
99	ESCL	Outputs clock signal to the EEPROM (IC308, pin 6).
100	CODE8	Output port for "CODE8" signal.

4-6-2 D/A CONVERTER (MAIN UNIT; IC303)

Pin number	Port name	Description
2	SQL	Outputs AF signals to the squelch circuit (IC3, pin 8).
3	MOD	Outputs modulation signals to the modulation circuit (D8).
10	TENC	Outputs CTCSS/DTCS signals.
11	BAL	Outputs deviation balance control signal.
14	BEPV	Outputs beep audio signals to the speaker via the AF amplifier (FRONT UNIT; IC201).
15	SIGNAL	Outputs AF signals to the speaker via the AF amplifiers (FRONT UNIT; IC201).
22	TONE	Outputs single tone signal.
23	REF	Outputs reference oscillator control signal.

4-6-3 D/A CONVERTER (MAIN UNIT; IC310)

Pin number	Port name	Description
1	T1	Outputs the bandpass filters (D18, D19) tuning signal.
2	T2	<ul style="list-style-type: none"> • While receiving: Outputs the bandpass filters (D15, D16) tuning signal. • While transmitting: Outputs the TX power control signal which selects TX output power of HIGH or LOW. The output signal is applied to the ALC amplifier (IC5, pin 1).
3	TXLVA	Outputs TX VCO lock voltage.
4	RXLVA	Outputs RX VCO lock voltage.

SECTION 5 ADJUSTMENT PROCEDURES

5-1 PREPARATION

When adjusting IC-F70DS/DT/S/D, the optional CS-F70/F1700 ADJ ADJUSTMENT SOFTWARE (Rev. 1.1 or later), OPC-966 JIG CABLE (modified OPC-966 CLONING CABLE; see illustration page 5-2) are required.

■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 7.2 V DC Current capacity : 3 A or more	Audio generator	Frequency range : 300–3000 Hz Measuring range : 1–500 mV
FM deviation meter	Frequency range : DC–300 MHz Measuring range : 0 to ±10 kHz	Attenuator	Power attenuation : 50 or 60 dB Capacity : 10 W
Frequency counter	Frequency range : 0.1–300 MHz Frequency accuracy : ±1 ppm or better Sensitivity : 100 mV or better	Standard signal generator (SSG)	Frequency range : 0.1–300 MHz Output level : 0.1 µV to 32 mV (−127 to −17 dBm)
Digital multimeter	Input impedance : 10 MΩ/V DC or more	AC millivoltmeter	Measuring range : 10 mV to 10 V
RF power meter	Measuring range : 1–10 W Frequency range : 100–300 MHz Impedance : 50 Ω SWR : Better than 1.2 : 1	Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–20 V
	External speaker	Input impedance : 8 Ω Capacity : 1 W or more	

■ SYSTEM REQUIREMENTS

- Microsoft® Windows® 98/98SE/Me/2000/XP
- RS-232C serial port (D-sub 9 pin)

■ ADJUSTMENT SOFTWARE INSTALLATION

- ① Quit all applications when Windows is running.
- ② Insert the CD into the appropriate CD drive.
- ③ Double-click the “Setup.exe” contained in the ‘CS-F70/F1700 ADJ’ folder in the CD drive.
- ④ The “Welcome to the InstallShield Wizard for CS-F70/F1700 ADJ” will appear. Click [Next>].
- ⑤ The “Choose Destination Location” will appear. Then click [Next>] to install the software to the destination folder. (e.g. C:\Program Files\Icom\CS-F70/F1700 ADJ)
- ⑥ After the installation is completed, the “InstallShield Wizard Complete” will appear. Then click [Finish].
- ⑦ Eject the CD.
- ⑧ Program group ‘CS-F70/F1700 ADJ’ appears in the ‘Programs’ folder of the start menu, and ‘CS-F70/F1700 ADJ’ icon appears on the desk top screen.

■ BEFORE STARTING SOFTWARE ADJUSTMENT

Clone the adjustment frequencies into the transceiver, and set the configuration using with the CS-F70/F1700 CLONING SOFTWARE before starting the software adjustment. Otherwise, the transceiver can not start software adjustment.

CAUTION: BACK UP the originally programmed memory data in the transceiver before programming the adjustment frequencies.

When program the adjustment frequencies into the transceiver, the transceiver's memory data will be overwritten and lose original memory data at the same time.

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■ STARTING SOFTWARE ADJUSTMENT

- ① Connect the transceiver and PC with OPC-966 JIG CABLE.
- ② Turn the transceiver power ON.
- ③ Boot up Windows, and click the program group ‘CS-F70/F1700 ADJ’ in the ‘Programs’ folder of the [Start] menu, then CS-F70/F1700 ADJ’s window appears.
- ④ Click ‘Connect’ on the CS-F70/F1700 ADJ’s window, then appears transceiver’s up-to-date condition.
- ⑤ Set or modify adjustment data as desired.

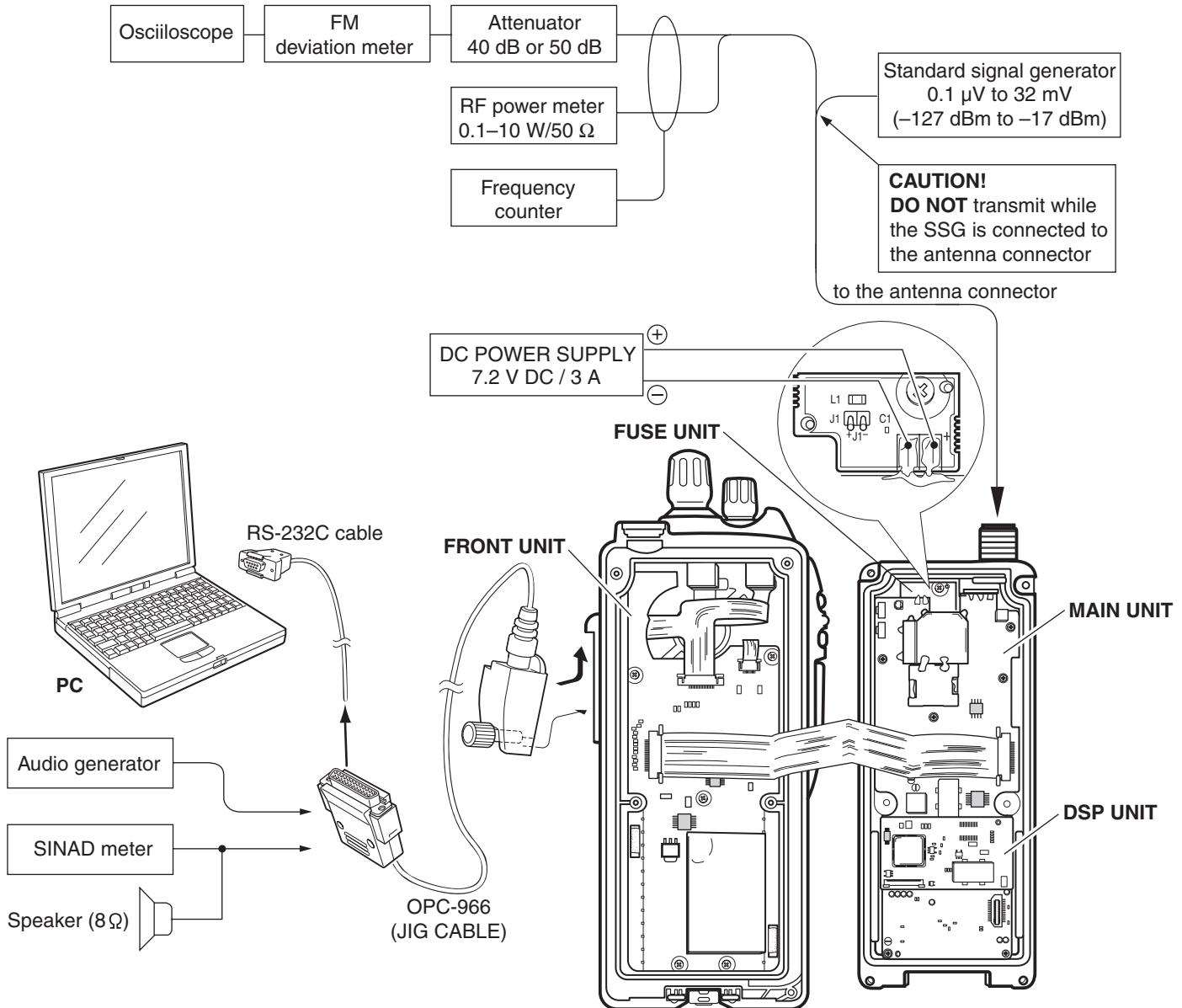
• ADJUSTMENT FREQUENCY LIST

CH	FREQUENCY	ADJUSTMENT ITEM
1	153.900 MHz	TX power : Low1 Mode : Wide
2	174.000 MHz	TX power : Low1 Mode : Narrow
3	155.000 MHz	TX power : High Mode : Wide
4	155.000 MHz	TX power : Low2 Mode : Wide
5	155.000 MHz	TX power : Low1 Mode : Wide
6	136.000 MHz	TX power : Low1 Mode : Wide
7	174.000 MHz	TX power : Low1 Mode : Wide
8	136.000 MHz	TX power : Low1 Mode : Narrow
9*	155.000 MHz	TX power : Low1 Mode : Digital Preamble Length [†] : 270
10*	136.000 MHz	TX power : Low1 Mode : Digital Preamble Length [†] : 270
11*	174.000 MHz	TX power : Low1 Mode : Digital
12	155.000 MHz	TX power : Low1 Mode : Wide CTCSS : 151.4 Hz
13	155.000 MHz	TX power : Low1 Mode : Narrow

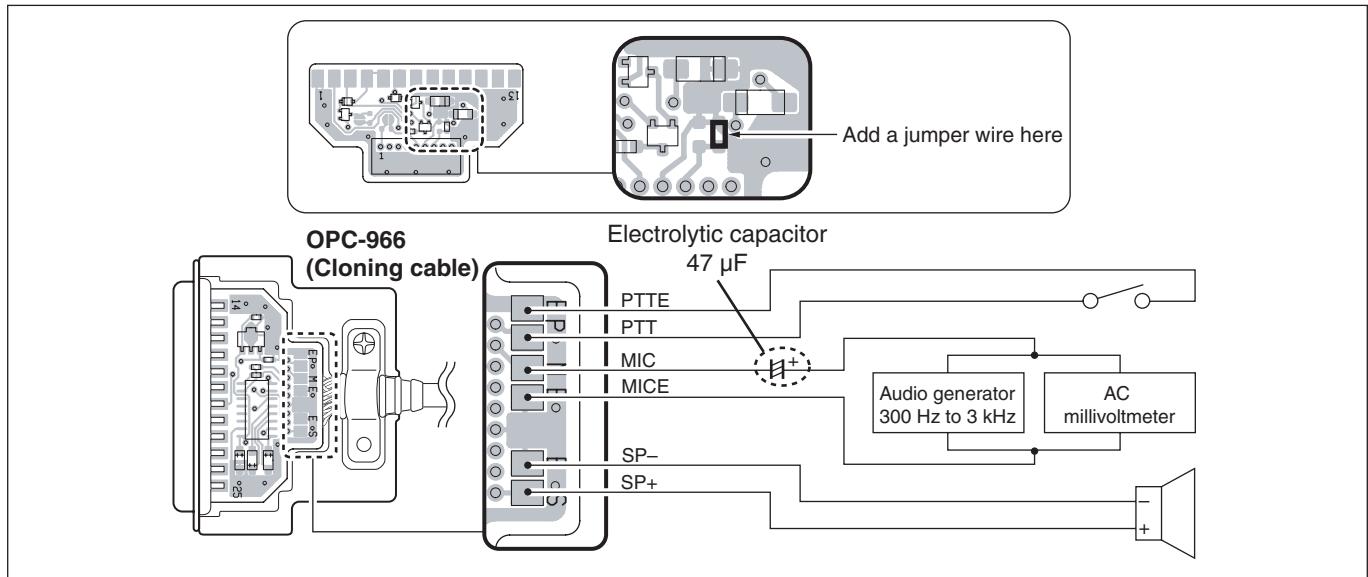
*; IC-F70DT/DS only

†; [USA-02] only

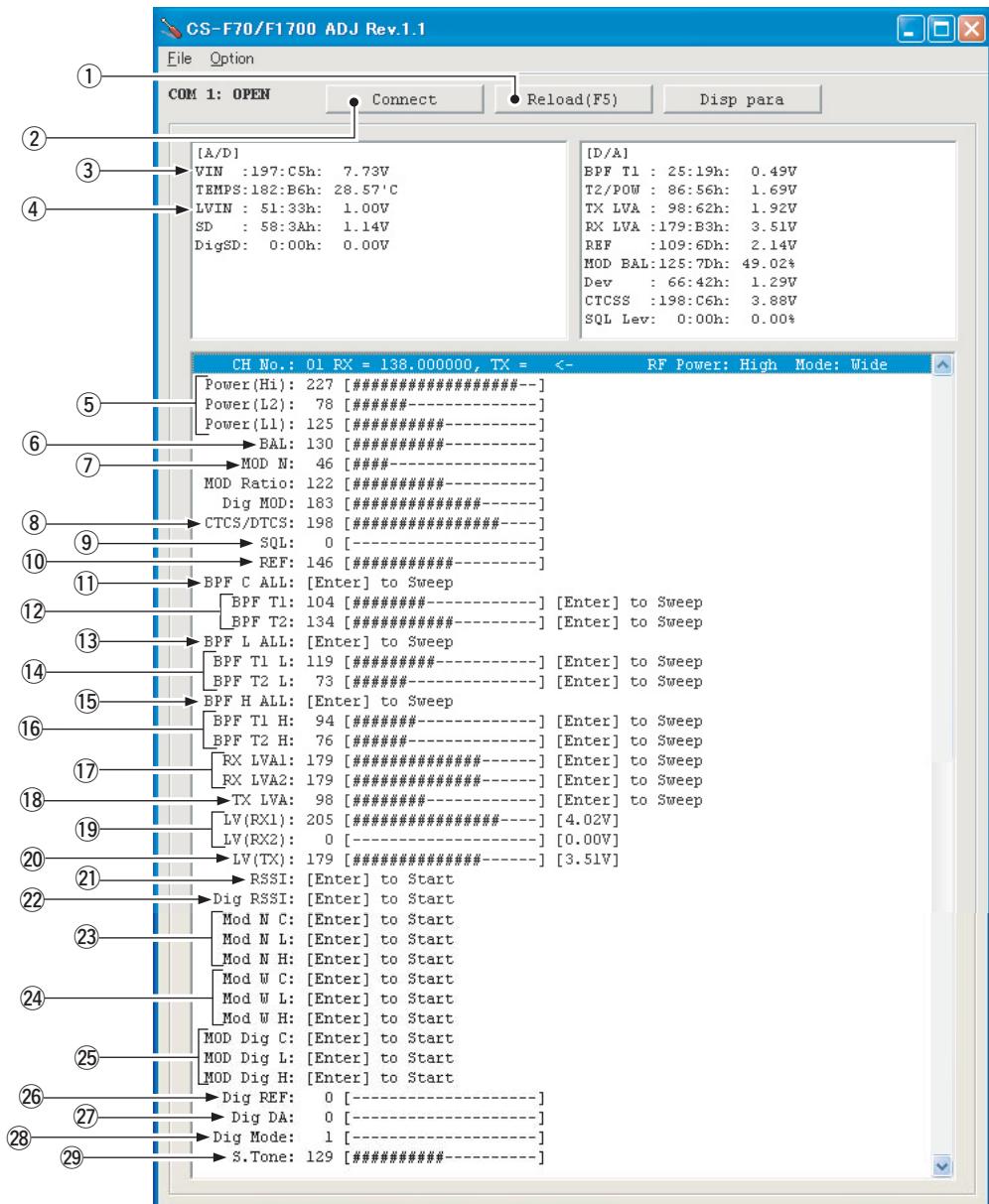
• CONNECTION



• JIG cable



• PC SCREEN EXAMPLE



NOTE: The above values for settings are example only.

Each transceiver has its own specific values for each setting.

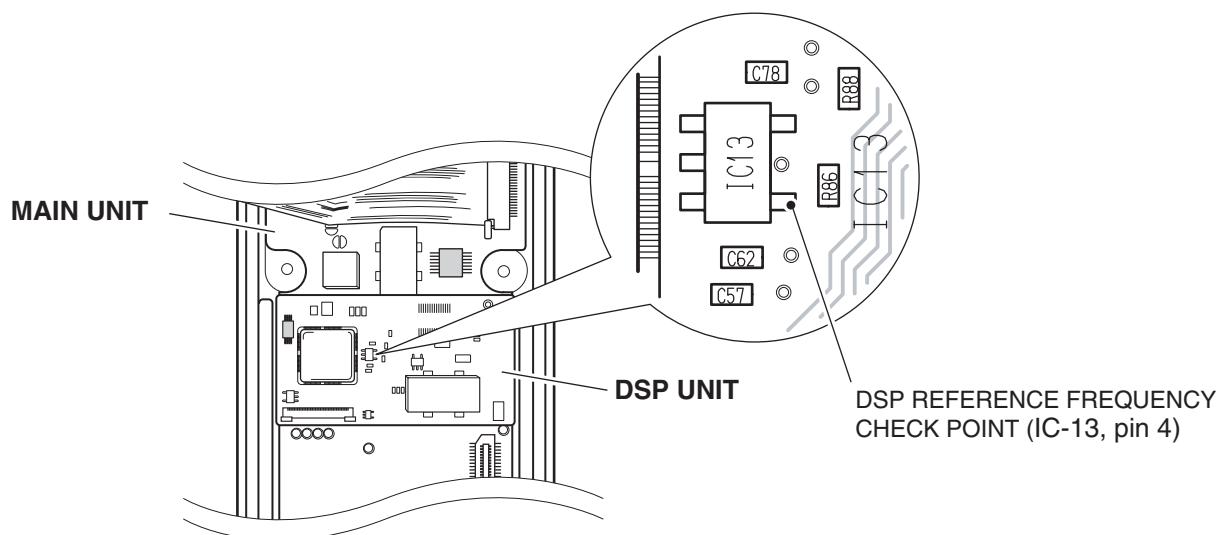
- | | | |
|-------------------------------------|--|-----------------------------|
| ①: Reload adjustment data | ⑪: Receive sensitivity for center (automatic) | ㉑: S-meter |
| ②: Transceiver's connection state | ⑫: Receive sensitivity for center (manual) | ㉒: S-meter (digital) |
| ③: Connected DC voltage measurement | ⑬: Receive sensitivity for low edge (automatic) | ㉓: Deviation (narrow) |
| ④: PLL lock voltage measurement | ⑭: Receive sensitivity for low edge (manual) | ㉔: Deviation (wide) |
| ⑤: RF output power | ⑮: Receive sensitivity for high edge (automatic) | ㉕: Deviation (digital) |
| ⑥: FM modulation balance | ⑯: Receive sensitivity for high edge (manual) | ㉖: DSP reference frequency |
| ⑦: FM modulation preset | ⑰: PLL lock voltage adjust for RX (manual) | ㉗: Base band center voltage |
| ⑧: CTCSS/DTCS deviation | ⑱: PLL lock voltage adjust for TX (manual) | ㉘: Digital mode |
| ⑨: Squelch level | ⑲: PLL lock voltage preset for RX (automatic) | ㉙: 2/5 TONE, DTMF deviation |
| ⑩: Reference frequency | ㉚: PLL lock voltage preset for TX (automatic) | |

5-2 SOFT WARE ADJUSTMENT

Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard

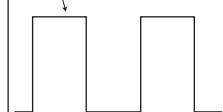
ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE
			UNIT	OPERATION	
PLL LOCK VOLTAGE [RX LVA1]	1	<ul style="list-style-type: none"> • Operating CH. : CH 2 • Preset [LV (RX1)] : 169 [3.30 V] • Receiving 	PC screen	Click [Reload (F5)] button, then check the "LVIN" item on the CS-F70/F1700 ADJ's screen.	3.3 V
[RX LVA2]	2	<ul style="list-style-type: none"> • Operating CH. : CH 1 • Preset [LV (RX2)] : 179 [3.50 V] • Receiving 			3.5 V
[TX LVA]	3	<ul style="list-style-type: none"> • Operating CH. : CH 2 • Preset [LV (TX)] : 179 [3.50 V] • Transmitting 			3.5 V
CONVENIENT: The PLL lock voltage can be adjusted automatically. Put the cursor on each items "RX LVA1"/"RX LVA2"/"TX LVA" and then push [ENTER] key of the connected PC's keyboard.					
PLL LOCK VOLTAGE	1	<ul style="list-style-type: none"> • Operating CH. : CH 2 • Receiving 	PC screen	Click [Reload (F5)] button, then check the "LVIN" item on the CS-F70/F1700 ADJ's screen.	3.2–3.4 V (Verify)
	2	<ul style="list-style-type: none"> • Operating CH. : CH 1 • Receiving 			3.4–3.6 V (Verify)
	3	<ul style="list-style-type: none"> • Operating CH. : CH 2 • Transmitting 			3.4–3.6 V (Verify)
REFERENCE FREQUENCY [REF]		<ul style="list-style-type: none"> • Operating CH. : CH 2 • Connect an RF power meter or 50 Ω dummy load to the antenna connector. • Transmitting 	Top panel	Loosely couple a frequency counter to the antenna connector.	174.000000 MHz ±100 Hz
DSP REFERENCE FREQUENCY* [Dig REF]		<ul style="list-style-type: none"> • Operating CH. : CH 9 • Receiving 	DSP unit	Connect a frequency counter to the pin 4 of IC13 on the DSP unit through a 1000 pF capacitor. (see the illust below)	12.288000 MHz
BASE BAND CENTER VOLTAGE* [Dig DA]		<ul style="list-style-type: none"> • Operating CH. : CH 9 • Receiving 	PC screen	Set the "Dig DA" item to 70.	

*: IC-F70DT/DS only



SOFTWARE ADJUSTMENT (Continued)

Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE
			UNIT	OPERATION	
OUTPUT POWER [Power (Hi)]	1	• Operating CH. : CH 3 • Transmitting	Top panel	Connect an RF power meter to the antenna connector.	5.0 W
[Power (L2)]	2	• Operating CH. : CH 4 • Transmitting			2.0 W
[Power (L1)]	3	• Operating CH. : CH 5 • Transmitting			1.0 W
MODULATION BALANCE [BAL]	1	• Operating CH. : CH 5 • Preset [MOD N] : 100 • No audio applied to the JIG cable. • Set an FM deviation meter as; HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P-P)/2 • Push [P0] while transmitting.	Top panel	Connect an FM deviation meter with an oscilloscope to the antenna connector through an attenuator.	Set to square wave form 
FM DEVIATION (NARROW) [MOD N C]	1	• Operating CH. : CH 13 • Connect an audio generator to the JIG cable and set as; : 1.0 kHz/150 mV rms • Set an FM deviation meter as; HPF : OFF LPF : 20 kHz De- emphasis : OFF Detector : (P-P)/2 • Transmitting			
(NARROW) [MOD N L]	2	• Operating CH. : CH 8 • Transmitting			
(NARROW) [MOD N H]	3	• Operating CH. : CH 2 • Transmitting			
(WIDE) [MOD W C]	4	• Operating CH. : CH 5 • Transmitting			
(WIDE) [MOD W L]	5	• Operating CH. : CH 6 • Transmitting			
(WIDE) [MOD W H]	6	• Operating CH. : CH 7 • Transmitting			

SOFTWARE ADJUSTMENT (Continued)

Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE
			UNIT	OPERATION	
DIGITAL DEVIATION* [MOD Dig C]	1	• Preset [Dig Mode] : 7	Top panel	Connect an FM deviation meter to the antenna connector through an attenuator.	± 2.83 to ± 2.87 kHz
	2	• Operating CH. : CH 9 • Set an FM deviation meter as; HPF : OFF LPF : 20 kHz De- emphasis : OFF Detector : (P-P)/2 • Transmitting			
	3	• Operating CH. : CH 10 • Transmitting			
	4	• Operating CH. : CH 11 • Transmitting			
DIGITAL DEVIATION* [MOD Dig C]	1	• Preset [Dig Mode] : 6	Top panel	Connect an FM deviation meter to the antenna connector through an attenuator.	± 0.91 to ± 1.01 kHz (Verify)
	2	• Operating CH. CH 9 • Transmitting			
	3	• Operating CH. CH 10 • Transmitting			
	4	• Operating CH. CH 11 • Transmitting			
CTCSS/DTCS DEVIATION [CTCSS/DTCS]	1	• Operating CH. : CH 12 • No audio applied to the JIG cable. • Set an FM deviation meter as; HPF : OFF LPF : 20 kHz De- emphasis : OFF Detector : (P-P)/2 • Transmitting	Top panel	Connect an FM deviation meter to the antenna connector through an attenuator.	± 0.68 to ± 0.72 kHz
2/5 TONE /DTMF DEVIATION [S.Tone]	1	• Operating CH. : CH 5 • No audio applied to the JIG cable. • Set an FM deviation meter as; HPF : OFF LPF : 20 kHz De- emphasis : OFF Detector : (P-P)/2 • Push [P3] while transmitting.	Top panel	Connect an FM deviation meter to the antenna connector through an attenuator.	± 1.50 kHz

*; [IC-F70DT/DS] only

SOFTWARE ADJUSTMENT (continued)

- Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE
		UNIT	LOCATION	
RX SENSITIVITY [BPF C]	<p>NOTE: Need to adjust "S-METER ADJUSTMENT" after "RX SENSITIVITY ADJUSTMENT" is adjusted. Otherwise, "S-METER ADJUSTMENT" will not be adjusted properly.</p> <p>1 • Operating CH : CH 5 • Connect the SSG to the antenna connector and set as; Frequency : 155.000 MHz Level : +20 dBμ[†] (-87 dBm) Modulation : 1 kHz Deviation : ±3.5 kHz • Receiving</p> <p>[BPF L] 2 • Operating CH : CH 6 Frequency : 136.000 MHz • Receiving</p> <p>[BPF H] 3 • Operating CH : CH 7 Frequency : 174.000 MHz • Receiving</p>	PC screen	Connect the SINAD meter with an 8 Ω load to the JIG cable.	Minimum distortion level
	<p>CONVENIENT: The BPF C/L/H can be adjustment automatically.</p> <p>①-1: Put the cursor on "BPF C/L/H ALL" and then push [ENTER] key. ①-2: The connected PC tunes BPF C/L/H to peak levels. or ②-1: Put the cursor on the one of "BPF C/L/H" as desired. ②-2: Push [ENTER] key to start tuning. ②-3: Repeat ①-1 and ②-2 to perform additional BPF tuning.</p>			
Digital RSSI* [Dig RSSI]	<p>1 • Operating CH. : CH 9 • Connect the SSG to the antenna connector and set as; Frequency : 155.000 MHz Level : -20 dBμ[†] (-127 dBm) Modulation : No modulation • Receiving</p>		Put the cursor on "Dig RSSI" and push the [ENTER] key to set the Digital RSSI level.	
S-METER [RSSI]	<p>1 • Operating CH. : CH 5 • Connect the SSG to the antenna connector and set as; Frequency : 155.000 MHz Level : +23 dBμ[†] (-84 dBm) Modulation : 1 kHz Deviation : ±3.5 kHz • Receiving</p> <p>2 • Set the SSG as; Level : -7dBμ[†] (-114 dBm) • Receiving</p>		Push the [ENTER] key on the connected computer's keyboard to set "S3" level.	
SQUELCH LEVEL [SQL]	<p>1 • Operating CH. : CH 5 • Connect the SSG to the antenna connector and set as; Frequency : 155.000 MHz Level : -14dBμ[†] (-121 dBm) Modulation : 1 kHz Deviation : ±3.5 kHz • Receiving</p>	Top panel	Connect speaker to the JIG cable.	Set the SQL level to close squelch. Then set SQL level at the point where the audio signals just appears.

*: [IC-F70DT/DS] only

[†]: The output level of the standard signal generator (SSG) is indicated as the SSG's open circuit.

SECTION 6 PARTS LIST

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
IC1	11300010100	S.I.C LMX2352TMX	B	8.3/75.8
IC2	1110005340	S.I.C NJM12902V-TE1	T	8/75.7
IC3	1110003490	S.I.C TA31136FN	B	14.6/57.6
IC4	1190002050	S.I.C SPM5001	B	31.4/78.3
IC5	1110002750	S.I.C TA75S01F (TE85R)	T	24.8/101.4
IC6	1130004200	S.I.C TC4S66F (TE85R)	B	17.7/85.4
IC12	1110005340	S.I.C NJM12902V-TE1	T	31.9/56.5
IC300	1130009700	S.I.C LC73872M-TRM	B	34.9/29.5
IC301	1110006220	S.I.C AK2346-E2	B	15/39.8
IC302	1130008230	S.I.C BU4053BCFV-E2	B	13.9/29.3
IC303	1190001350	S.I.C M62364FP 600D	T	20.2/71.7
IC304	1110006260	S.I.C BD5242G-TR	B	4.7/8.6
IC305	1130008230	S.I.C BU4053BCFV-E2	B	33.4/66.4
IC307	1140010190	S.I.C HD64F2268TF20	B	20.2/15
IC308	1140009240	S.I.C HN58X24128FPI	B	38.2/17.7
IC310	1190001340	S.I.C M62334FP 600C	T	32.5/84.4
IC311	1180002270	S.REG TK11250CMCL	B	8.6/119.6
IC312	1190001860	S.I.C EW-460-FT	B	30.1/43.8
IC313	1130006220	S.I.C TC4W53FU (TE12L)	T	8.5/38.2

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
D31	1790001250	S.DIO MA2S111-(TX)	T	26.2/105.3
D301	1160000050	S.DIO DAP202U T106	T	33.6/26
D302	1160000050	S.DIO DAP202U T106	B	32.4/5.4
D303	1160000050	S.DIO DAP202U T106	T	39.7/27
D304	1160000050	S.DIO DAP202U T106	T	36.5/27.3
D306	1730002320	S.ZEN MA8051-M (TX)	B	11.1/5.2
D307	1790001260	S.DIO MA2S077-(TX)	B	9/24.5
D308	1790001250	S.DIO MA2S111-(TX)	B	21.9/27.1
D309	1790001250	S.DIO MA2S111-(TX)	T	37.8/29.3
D310	1750000270	S.DIO 1SS301 (TE85R)	B	35.9/5
D311	1750000270	S.DIO 1SS301 (TE85R)	B	11.3/7.5
D312	1790001250	S.DIO MA2S111-(TX)	B	27.4/44.7
D313	1160000050	S.DIO DAP202U T106	B	23.3/3
FI1	2020001930	S.CER CFWCA450KFFA-R0	T	21.5/57.1
FI2	2020002120	S.CER CFWCA450KGFA-R0	B	28.2/56.7
FI3	2030000410	S.MLH FL-380 MFT46.3P	B	20.3/69.6
X1	6050012060	S.XTL CR-796 (15.300 MHz)	B	5.4/68.4
X2	6070000190	S.DCR CDBCB450KCAY24-R0	T	12.5/55.5
X300	6050012100	S.XTL CR-800 (3.579545 MHz)	B	34.6/38.3
X301	6050012090	S.XTL CR-799 (3.6864 MHz)	B	5.4/39.2
X302	6050012110	S.XTL CR-803 (19.6608 MHz)	B	7.4/19.5
L1	6200004930	S.COL MLF1608E 8R2K-T	B	9.7/68.9
L2	6200011250	S.COL LLQ1608-A18NG	B	11.5/85.9
L3	6200007170	S.COL MLF1608A 3R3K-T	T	23.2/84.4
L4	6200007170	S.COL MLF1608A 3R3K-T	T	10.9/86.7
L6	6200008090	S.COL LQW2BHN68NJ01L	T	22.3/86.6
L7	6200003640	S.COL MLF1608E 100K-T	T	12.7/92.5
L8	6200003640	S.COL MLF1608E 100K-T	T	26.1/87.1
L9	6200011110	S.COL 0.42-2.00-9TL 80.2N	T	12.1/95.7
L10	6200007760	S.COL LQW2BHN82NJ01L	T	25.9/90.3
L11	6200009180	S.COL ELJRE R10J-F3	T	24.3/96.4
L12	6200011240	S.COL LLQ1608-A33NG	B	12.4/94.7
L13	6200011280	S.COL C1608CB-R10G	B	20.4/99.2
L14	6200005740	S.COL ELJRE 47NG-F	B	13.1/102.9
L15	6200003590	S.COL EXCCL3225U1	B	15.9/117.1
L16	6200005690	S.COL ELJRE 18NG-F	T	16.6/115.7
L17	6200008210	S.COL 0.45-1.5-5TL 23.2N	B	21.2/117.7
L18	6200009710	S.COL 0.30-0.9-4TL 10.5N	B	25.2/117.8
L19	6200008490	S.COL 0.30-0.9-3TR 7.5N	B	30.7/117.5
L20	6200008280	S.COL 0.30-1.7-7TL 50N	B	32.4/111
L21	6200002860	S.COL NL 252018T-4R7J	B	33.3/106
L22	6200009800	S.COL 0.26-1.1-7TR 30N	B	38.3/112.7
L23	6200008580	S.COL 0.30-1.4-6TL 32N	B	36.8/117.2
L24	6200003540	S.COL MLF1608D R22K-T	B	6.9/63.2
L25	6200004480	S.COL MLF1608D R82K-T	B	7.8/61
L26	6200002690	S.COL MLF1608A 1R0M-T	B	11.5/63.3
L27	6200004660	S.COL MLF1608A 1R8K-T	B	20.2/64.6
L29	6200004790	S.COL MLF1608D R47K-T	B	20.9/75.5
L30	6130003000	S.COL 617DB-1714=P3	B	26.1/79.2
L31	6130003000	S.COL 617DB-1714=P3	B	31.4/85.1
L32	6200004780	S.COL MLF1608A 1R5K-T	B	12.8/63.3
L33	6130003000	S.COL 617DB-1714=P3	B	36.6/79.2
L34	6200011260	S.COL C1608CB-15NG	B	30.3/93.5
L35	6200011260	S.COL C1608CB-15NG	B	29.5/96.3
L37	6200009920	S.COL C2012C-R10G	B	33.4/96.5
L38	6200011050	S.COL C2012C-R12G	B	36.6/100
L39	6200011050	S.COL C2012C-R12G	B	38.3/103
L40	6200011150	S.COL C1608CB-68NG	B	36.5/85.6
L41	6200010400	S.COL ELJRE 39NJ-F	B	36/105.8
L42	6200008280	S.COL 0.30-1.7-7TL 50N	B	38.1/106.4
L43	6200007170	S.COL MLF1608A 3R3K-T	B	15.1/91
L44	6200007170	S.COL MLF1608A 3R3K-T	B	25.1/88
L45	6200011130	S.COL C1608CB-12NG	B	39.6/82
L46	6200004660	S.COL MLF1608A 1R8K-T	B	13.1/80.2
L47	6200007170	S.COL MLF1608A 3R3K-T	T	12.1/86.7
L48	6200007170	S.COL MLF1608A 3R3K-T	B	16.3/89
L49	6200010100	S.COL C2012C-33NG	B	39.3/87.2
L50	6200003640	S.COL MLF1608E 100K-T	T	14.5/87.6
L51	620001120	S.COL 0.40-2.00-10TL 90.5N	T	18.2/86.3
L52	6200011150	S.COL C1608CB-68NG	T	36.5/87
L53	6200011140	S.COL C1608CB-39NG	T	38.4/87.5
L54	6200011150	S.COL C1608CB-68NG	T	36.5/89.7
L55	6200010310	S.COL C2012C-27NG	B	37.1/91.7
L56	6200011230	S.COL LLQ1608-A22NG	B	8.5/85
L57	6200011230	S.COL LLQ1608-A22NG	B	8.5/82.4
L58	6200011060	S.COL C1608CB-18NG	B	21.8/100.3
L60	6200009890	S.COL C2012C-82NG	T	37.9/108.6
L61	6200009920	S.COL C2012C-R10G	B	42.1/77.3
L301	6200002860	S.COL NL 252018T-4R7J	B	25.7/28.8

M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)

S.=Surface mount

[DSP UNIT] (IC-F70DT/DS only)

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
R65	7030004970	S.RES ERJ2GEJ 470 X (47 Ω)	T	25.7/27.1
R66	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	B	7.3/19.2
R67	7030007290	S.RES ERJ2GEJ 222 X (2.2 kΩ)	T	22/27.3
R68	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	T	20.8/29.1
R70	7030008290	S.RES ERJ2GEJ 183 X (18 kΩ)	T	9.1/10.2
R71	7030005600	S.RES ERJ2GEJ 273 X (27 kΩ)	T	8.2/10.2
R72	7030008290	S.RES ERJ2GEJ 183 X (18 kΩ)	T	7.3/10.2
R73	7030005600	S.RES ERJ2GEJ 273 X (27 kΩ)	T	6.4/9.2
R74	7030005600	S.RES ERJ2GEJ 273 X (27 kΩ)	T	5.5/9.2
R75	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	T	9.3/12.4
R76	7030007340	S.RES ERJ2GEJ 153 X (15 kΩ)	T	8.4/12.4
R77	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	T	7.5/12.9
R78	7030007340	S.RES ERJ2GEJ 153 X (15 kΩ)	T	6.6/12.7
R79	7030007340	S.RES ERJ2GEJ 153 X (15 kΩ)	T	5.7/12
R80	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	B	20.7/35.9
R82	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	3.5/17.2
R83	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	B	2.1/38.6
R85	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	B	4.3/38.8
R86	7030005010	S.RES ERJ2GEJ 681 X (680 Ω)	B	12.1/20.3
R87	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	10.7/18.5
R88	7030004970	S.RES ERJ2GEJ 470 X (47 Ω)	B	9.8/19.8
R89	7030010040	S.RES ERJ2GEJ-JPW	T	3.3/37.4
R90	7030008370	S.RES ERJ2GEJ 561 X (560 Ω)	T	22/28.9
R91	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	23.4/25.7
R92	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	23.5/24.8
R93	7030010040	S.RES ERJ2GEJ-JPW	T	22.2/24
R94	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	7.8/19.8
R95	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	17.1/19.6
R96	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	T	1.6/11.8
R97	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	T	1.9/18.6

[DSP UNIT] (IC-F70DT/DS only)

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
C66	4550007030	S.TAN TEESVP 0J 106M8R	T	22.4/12.6
C67	4030017490	S.CER C1608 JB 1A 105K-T	T	20/17.2
C68	4030017460	S.CER ECJ0EB1E102K	T	1.2/26.5
C69	4030017460	S.CER ECJ0EB1E102K	T	1.6/38.1
C70	4030017490	S.CER C1608 JB 1A 105K-T	T	20.9/37.9
C71	4030017460	S.CER ECJ0EB1E102K	T	19.2/37.5
C72	4030016930	S.CER ECJ0EB1A104K	B	24.7/19.3
C73	4030016930	S.CER ECJ0EB1A104K	T	25.7/38.9
C74	4030017620	S.CER ECJ0EC1H100C	T	23.3/32.1
C75	4030016930	S.CER ECJ0EB1A104K	T	24.5/32.6
C76	4030017460	S.CER ECJ0EB1E102K	B	4.9/18.8
C77	4030017460	S.CER ECJ0EB1E102K	T	24.8/27.1
C78	4030017460	S.CER ECJ0EB1E102K	B	9.4/21.8
C79	4030017460	S.CER ECJ0EB1E102K	T	18.9/38.7
C80	4030017460	S.CER ECJ0EB1E102K	T	9.3/21.3
C81	4030017460	S.CER ECJ0EB1E102K	T	10.3/13.3
C82	4550007070	S.TAN TEESVP 1A 475M8R	T	2.8/21.9
C83	4030016790	S.CER ECJ0EB1C103K	B	17.4/39.7
C84	4030016930	S.CER ECJ0EB1A104K	T	4.9/21.5
C85	4030016930	S.CER ECJ0EB1A104K	T	2.5/23.3
C86	4030017460	S.CER ECJ0EB1E102K	B	1.2/37.9
C88	4030017730	S.CER ECJ0EB1E471K	B	1.4/23.1
C89	4030017490	S.CER C1608 JB 1A 105K-T	B	2.9/21.9
C90	4030017730	S.CER ECJ0EB1E471K	B	1.5/24.8
C91	4030017730	S.CER ECJ0EB1E471K	B	4.8/4.9
C92	4030016930	S.CER ECJ0EB1A104K	T	21.8/30.5
C93	4030017640	S.CER ECJ0EC1H150J	T	23.3/27.5
C94	4030016930	S.CER ECJ0EB1A104K	T	22.2/25.6
J1	6510018440	S.CNR AXN430C330P	T	13.2/4.3

[CHASSIS UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
J1	6910015860	CNR IMSA-6277S-02A-G		
J2	6910016780	CNR ANT CONNECTOR-105		
SP1	2510001300	SP 036D0801C <FG>		
W1	8900013740	CBL OPC-1429		
W2	8900010960	CBL OPC-1129		

[VR BOARD]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
R1	7210003200	VAR TP76N937N-16.5F-10KA-2803		
DS1	5040003170	LED UW3804X		
S1	2250000500	ECR TP70TF5164S-20F-2803		

[FUSE BOARD]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
L1	6200006190	S.COL BLM21PG300SN1D	T	7.5/6.5
C1	4030017460	S.CER ECJ0EB1E102K	T	10.5/2.9
J1	6910015880	CNR IMSA-9230B-1-02Z141-T		

M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)
S.=Surface mount

SECTION 7 MECHANICAL PARTS AND DISASSEMBLY

[MAIN UNIT]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
S3	2260002840	Switch SKHLLFA010	1
MP1	8410002530	2681 PA heatsink	1
MP2	8510016880	2803 VCO case	1
MP3	8510016870	2803 VCO cover	1
MP4	6910014760	Plate OG-503040	1
MP5	8510016900	2803 PA shield	1
MP6	8930066240	Sponge (IM)	1

[DSP UNIT] (IC-F70DT/DS only)

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
MP1	8930059940	Sponge (HF)	1

[FUSE BOARD]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
J1	6910015880	Connector IMSA-9230B-1-02Z141-T	1

[ANT BOARD]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
MP1	8930065180	2803 ant plate	1

[VR BOARD]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
R1	7210003200	Variable resistor TP76N937N-16.5F-10KA-2803	1
S1	2250000500	Encoder TP70TF5164S-20F-2803	1
DS1	5040003170	LED UW3804X	1
EP1	0910059082	Cable B 6224B	1
MP1	8930057690	O ring (AQ)	2

Screw abbreviations

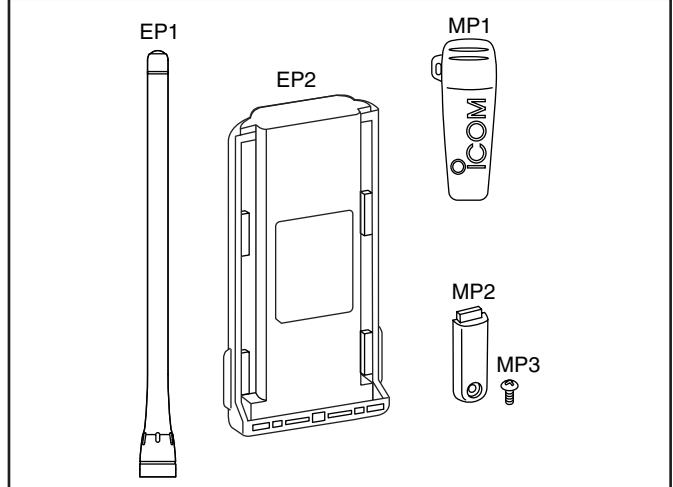
BT, B0: Self-tapping
 PH: Pan head FH: Flat head
 ZK: Black SUS: Stainless
 NI-ZU: Nickel-Zinc

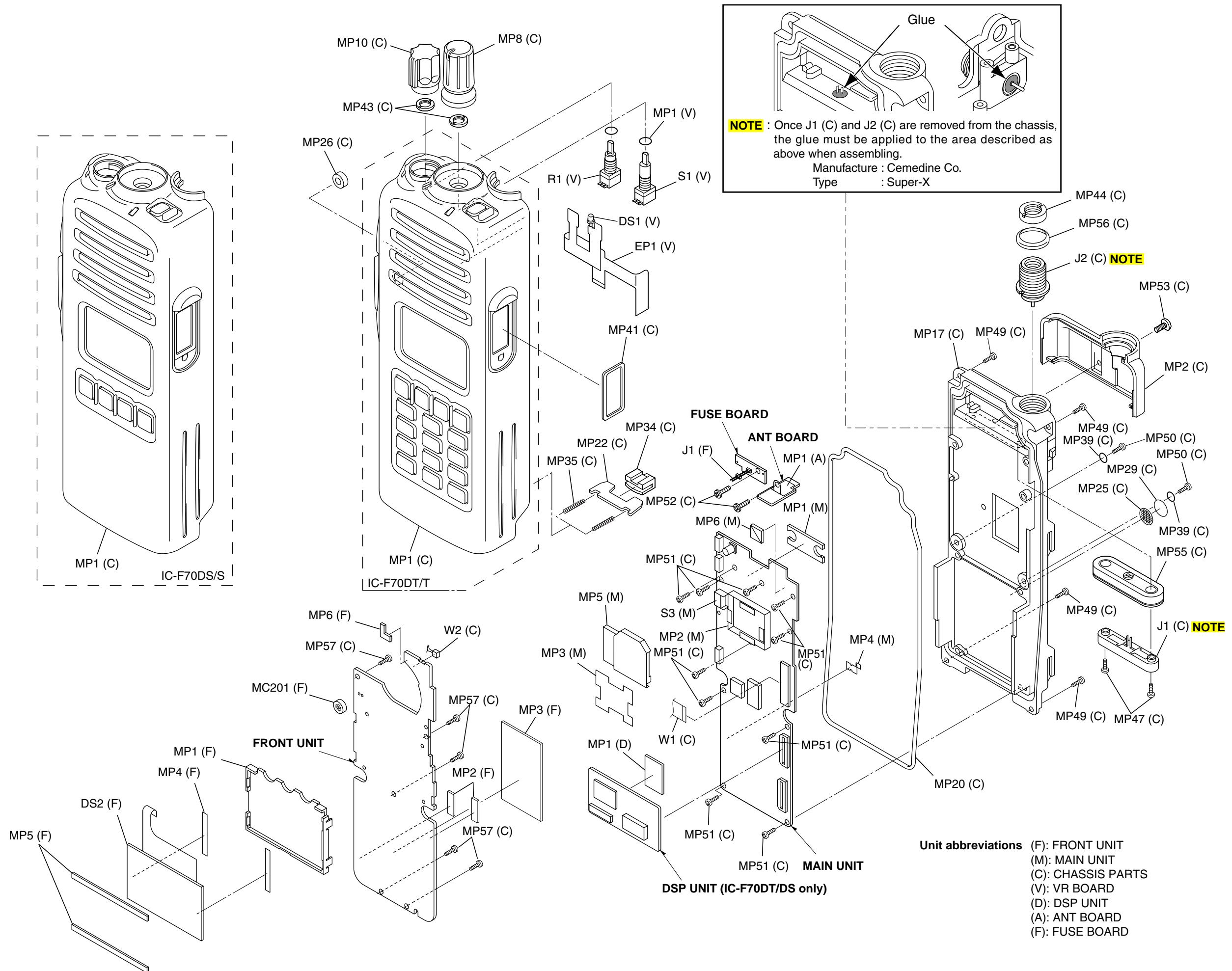
[ACCESORIES]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
EP1	Optional product	Antenna FA-SC55V-1	1
EP2	Optional product	Battery BP-235	1
MP1	Optional product	Belt clip MB-94	1
MP2	8210021470	2803 side panel	1
MP3	8810010430	Screw truss M3 × 5 SUS SSBC	1

[FRONT UNIT]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
DS2	5030002830	LCD M4-0078TAY-2	1
MC201	7700002310	Microphone EM-140	1
MP1	8210021460	2803 reflector	1
MP2	8930061120	Shield sponge (AA)	2
MP3	8930066040	Sponge (IK)	1
MP4	8950004430	Double coated tape (O)	2
MP5	8930062540	Sponge (HO)	2
MP6	8930066250	2803 sponge	1





SECTION 8 SEMICONDUCTOR INFORMATION

• TRANSISTORS AND FET'S

2SA1577 T106 Q (Symbol: HQ)	2SB1132 T100 Q (Symbol: BAQ)	2SC4081 T106 R (Symbol: BR)	2SC4116 BL (Symbol: LL)	2SC4116 Y (Symbol: LY)
2SC4215 Y (Symbol: QY)	2SC4226 T1 R25 (Symbol: R25)	2SC5107 O (Symbol: MFO)	2SC5110 O (Symbol: MGO)	2SK1771 (Symbol: UB)
2SK1829 (Symbol: K1)	2SK880 Y (Symbol: XY)	3SK293 (Symbol: UF)	DTA144 EE TL (Symbol: 16)	DTB123 EK T146 (Symbol: F12)
DTC144 EE TL (Symbol: 26)	DTC144EUA T106 (Symbol: 26_)	RD01MUS1 (Symbol: K2)	RD07MVS1 (Symbol: RD07MVS1)	RSR025N03 (Symbol: QY)
TPC6103 (Symbol: S3C)	UMG2N (Symbol: G2)	XP1214 (Symbol: 9H)	XP6501 AB (Symbol: 5N)	

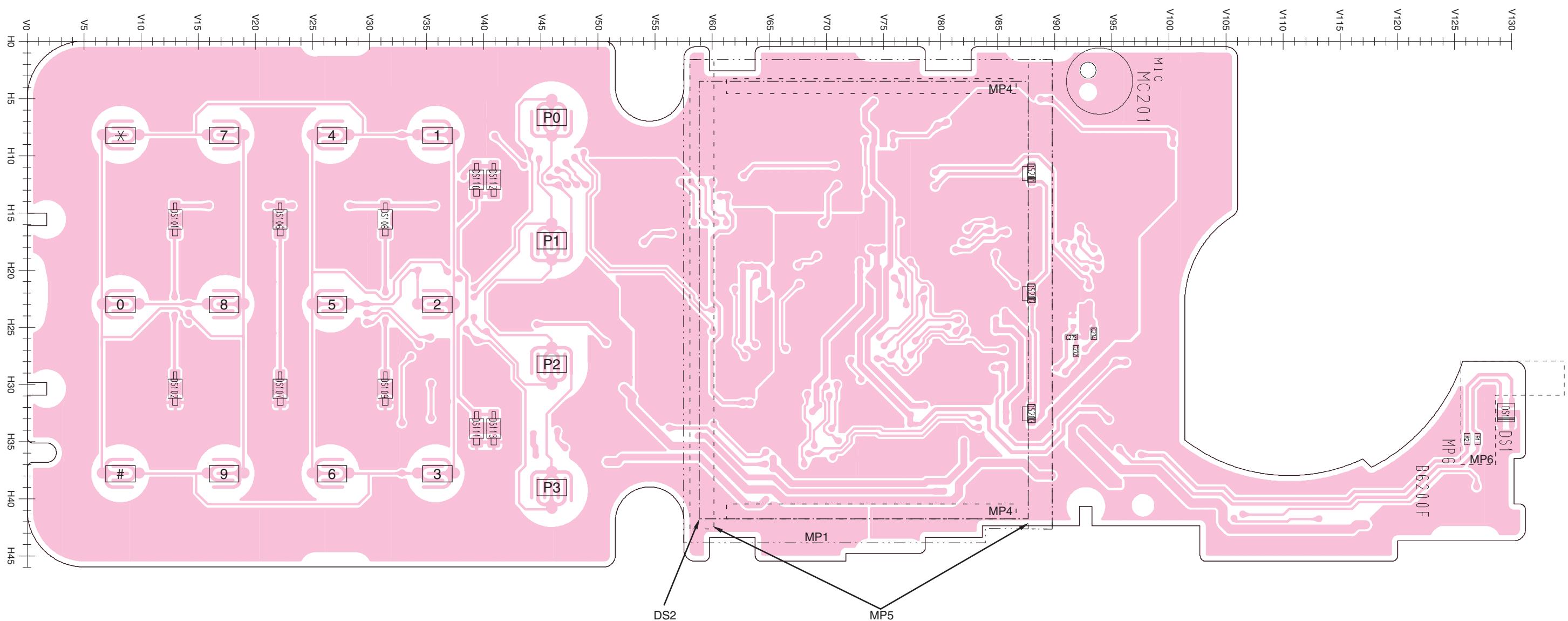
• DIODES

1SS301 (Symbol: B3)	1SV239 (Symbol: TC)	1SV284 (Symbol: TL)	1SV307 (Symbol: TX)	DAN235E TL (Symbol: M)
DAP202 U T106 (Symbol: P)	DAP222 TL (Symbol: P)	HVC350B (Symbol: B0)	HVC375B (Symbol: B8)	HVC376B (Symbol: B9)
MA2S077 (Symbol: S)	MA2S111 (Symbol: A)	MA2S728 (Symbol: B)	MA8051 M (Symbol: 5-1)	NNCD6.2G (Symbol: 62G)
RB706F-40 T106 (Symbol: 3J)				

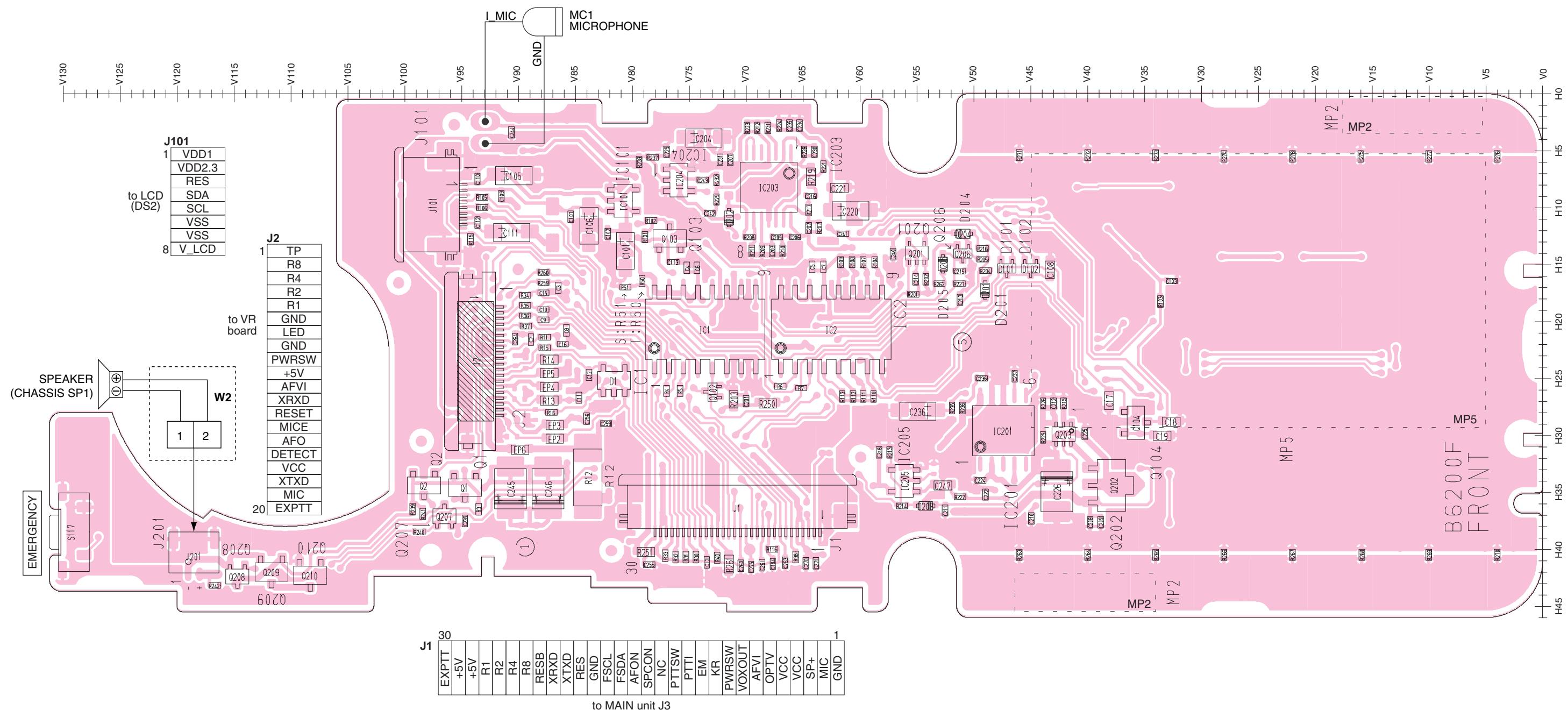
SECTION 9 BOARD LAYOUTS

9-1 FRONT UNIT

- TOP VIEW

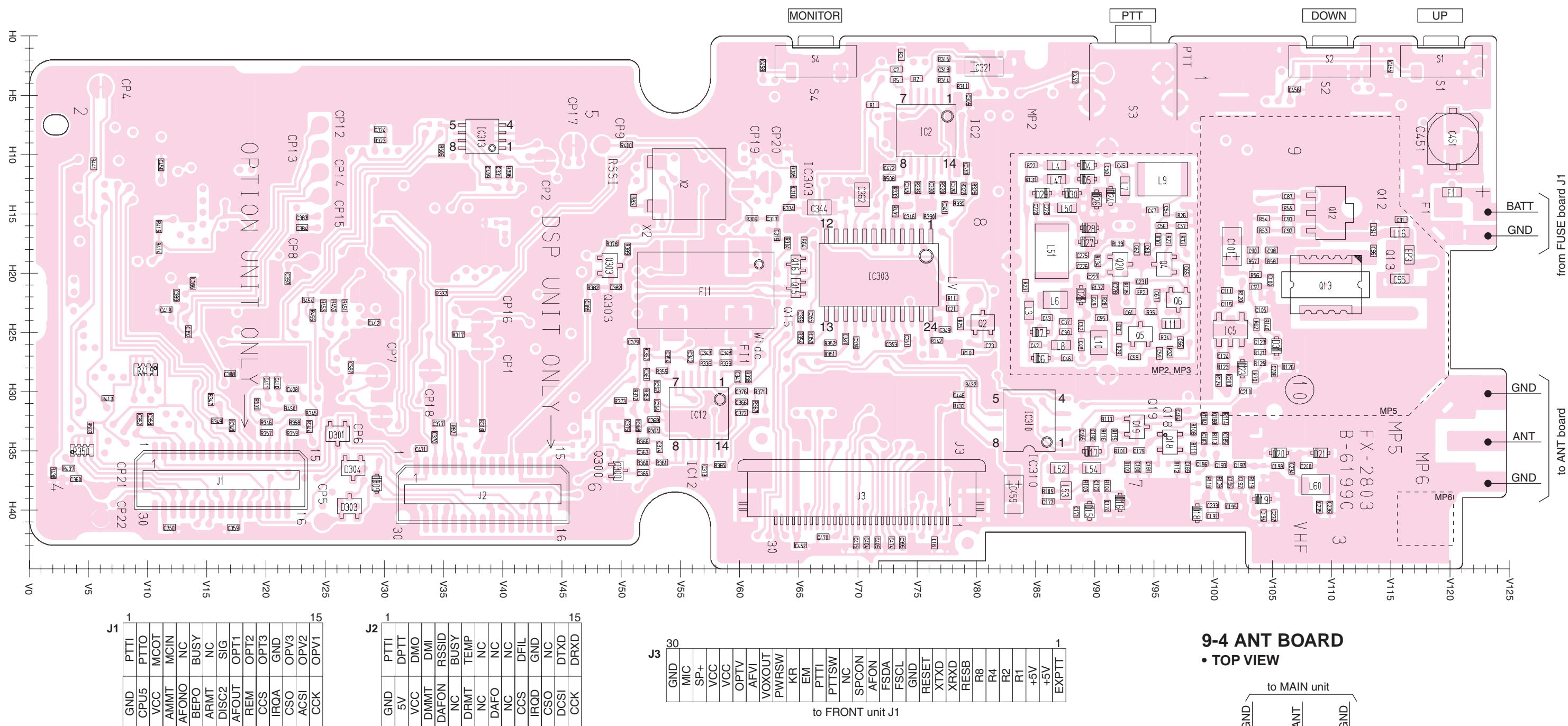


• BOTTOM VIEW (FRONT UNIT)



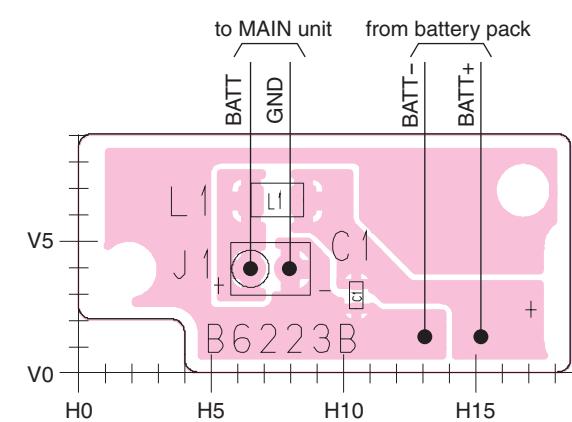
9-2 MAIN UNIT

• TOP VIEW



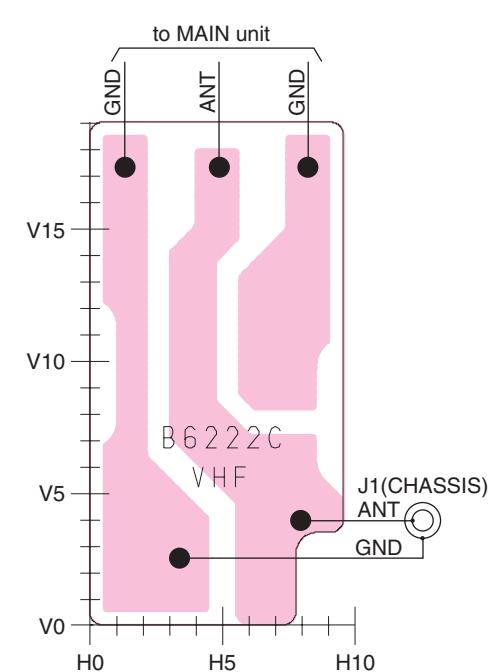
9-3 FUSE BOARD

• TOP VIEW

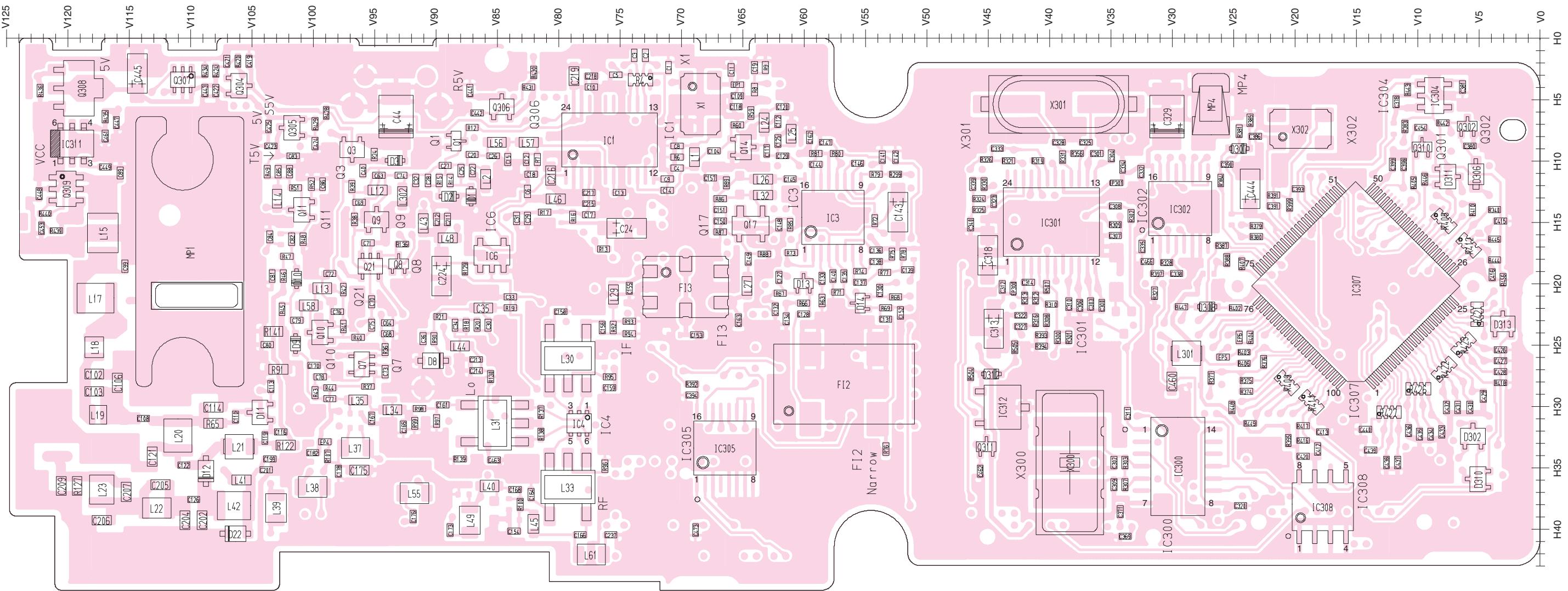


9-4 ANT BOARD

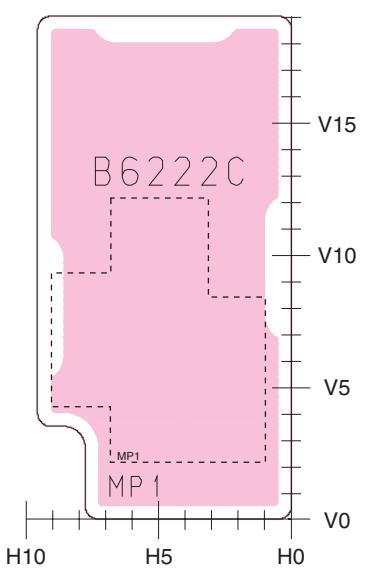
• TOP VIEW



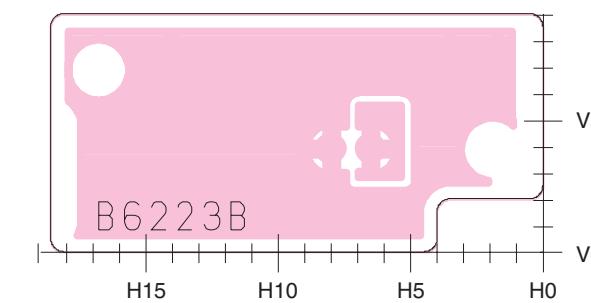
• BOTTOM VIEW (MAIN UNIT)



• BOTTOM VIEW (ANT BOARD)

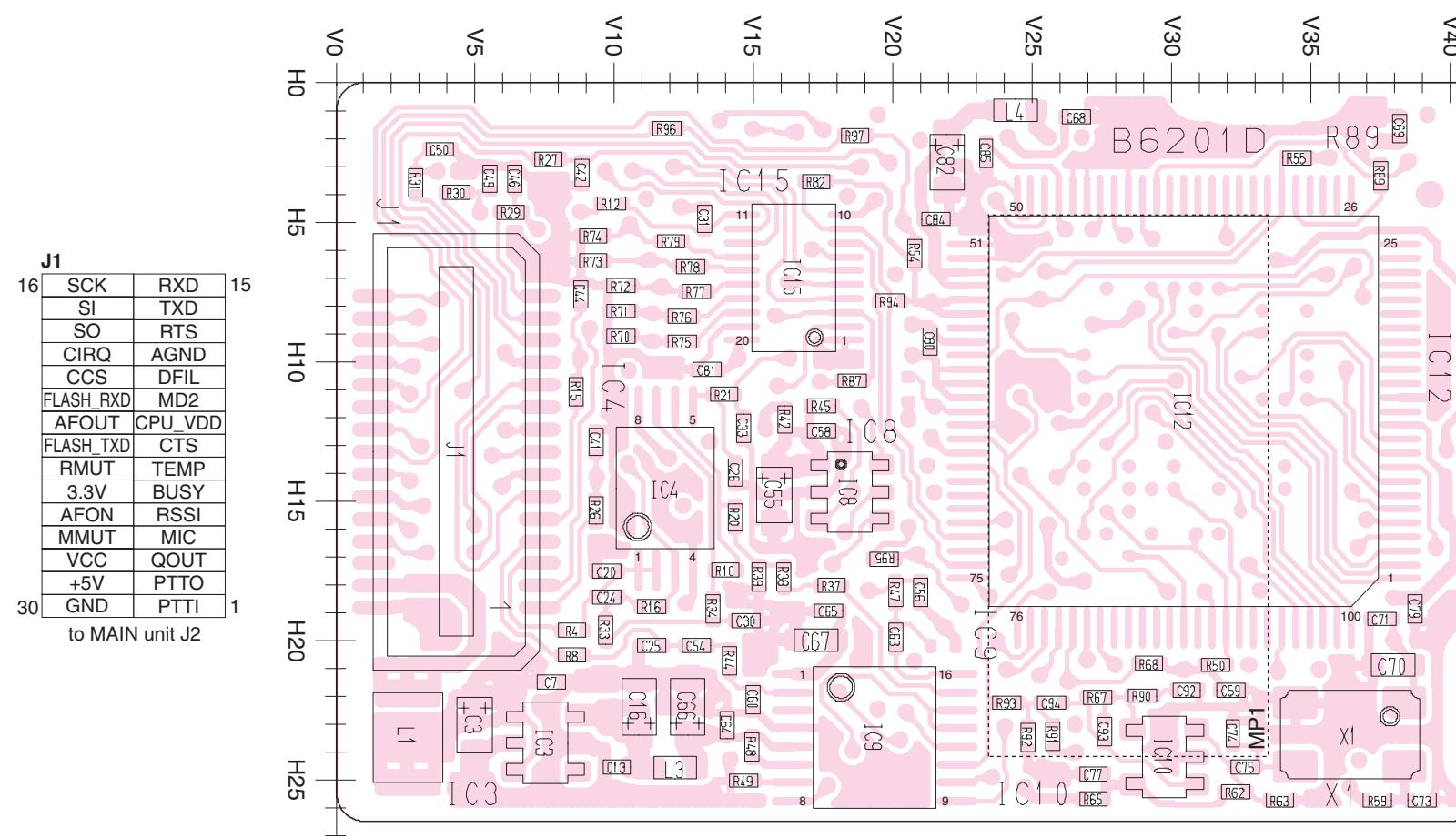


• BOTTOM VIEW (FUSE BOARD)

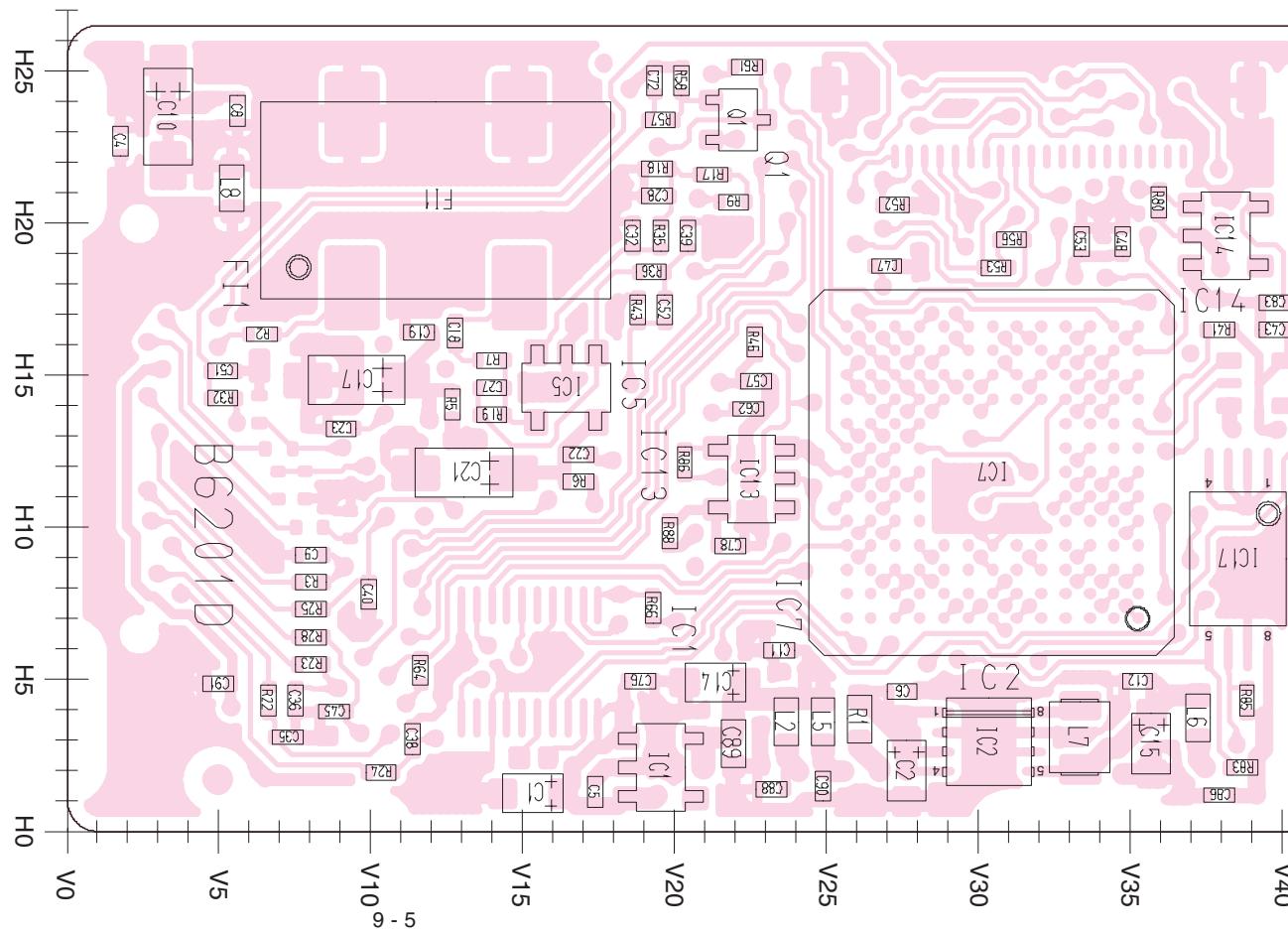


9-5 DSP UNIT (IC-F70DT/DS only)

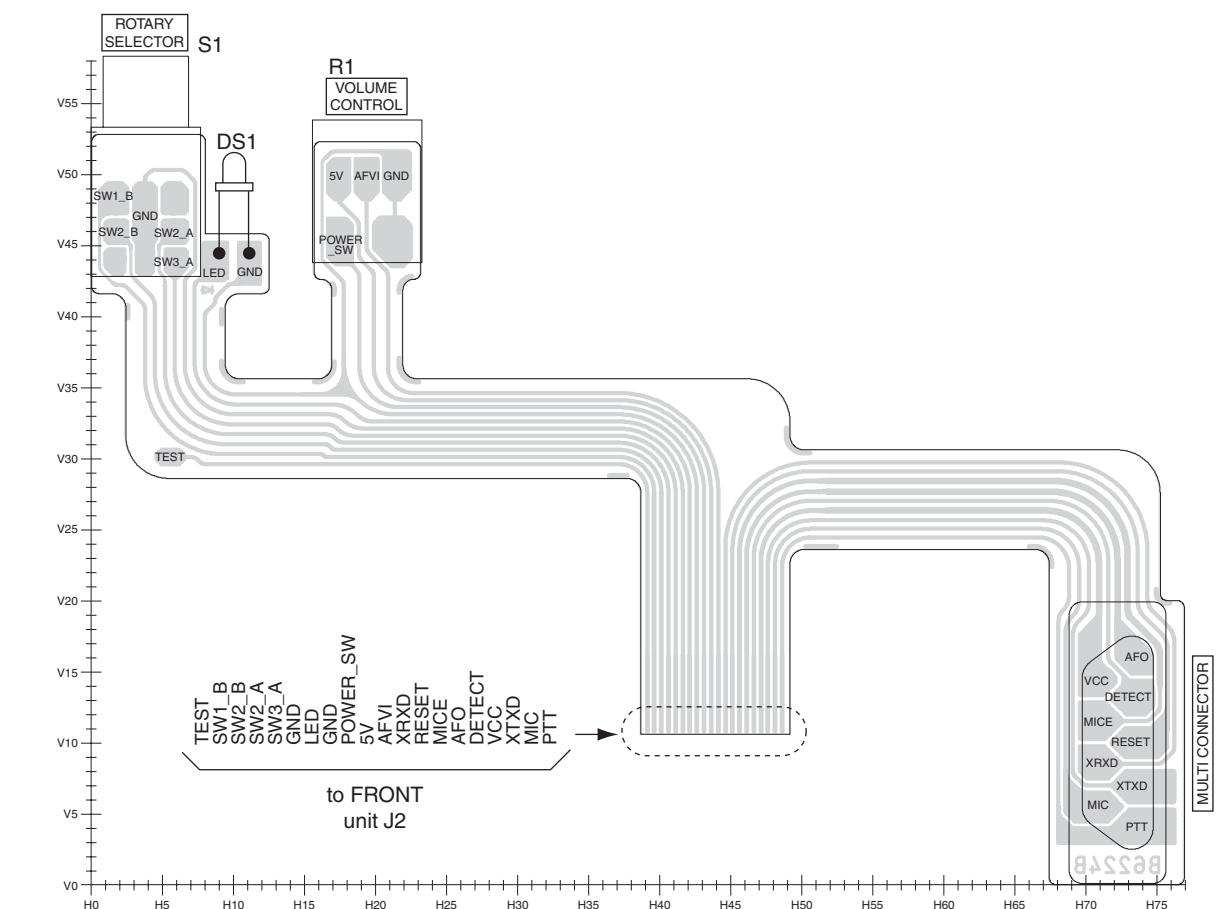
- TOP VIEW



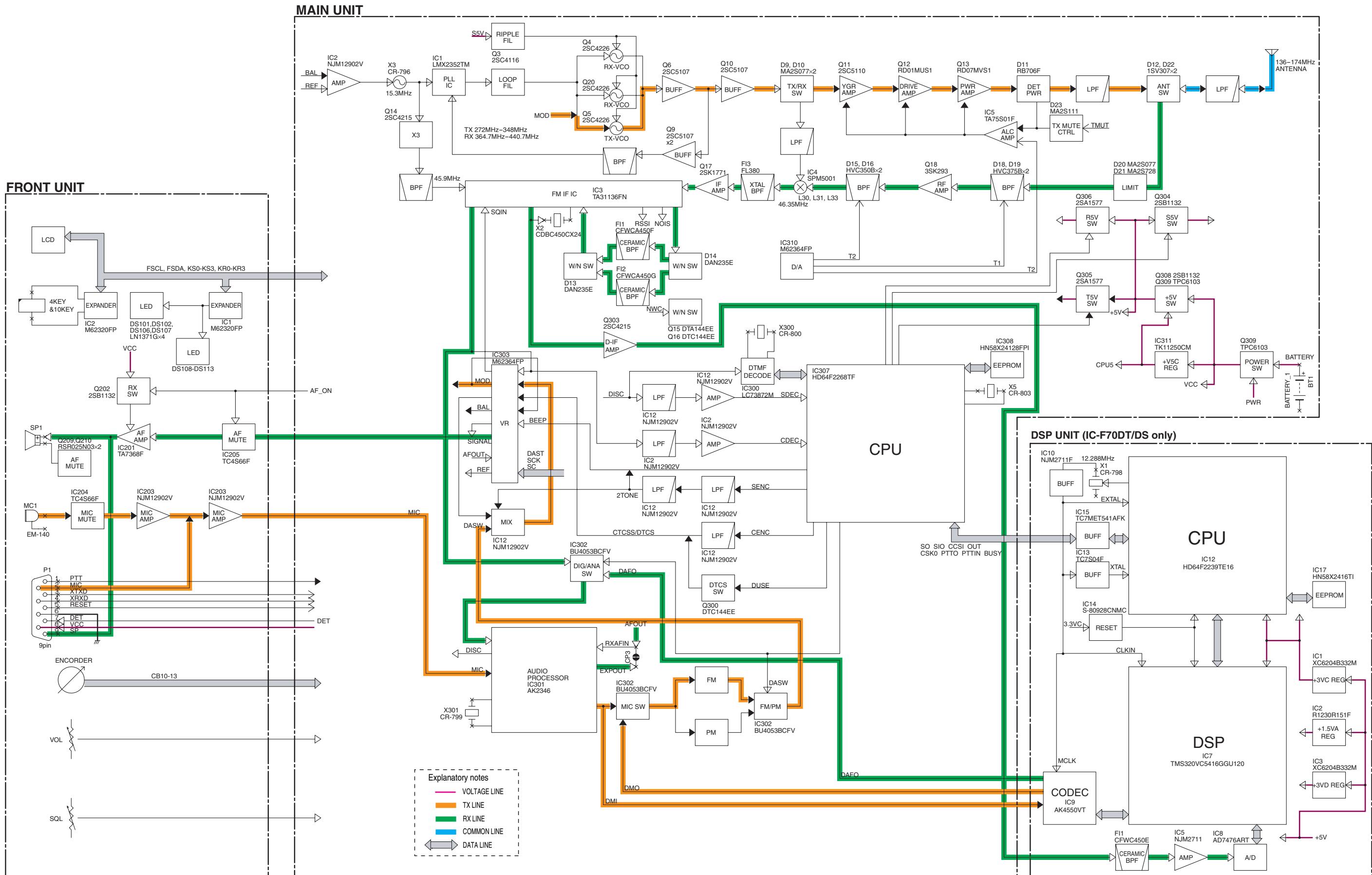
- BOTTOM VIEW (DSP UNIT)



9-6 VR BOARD

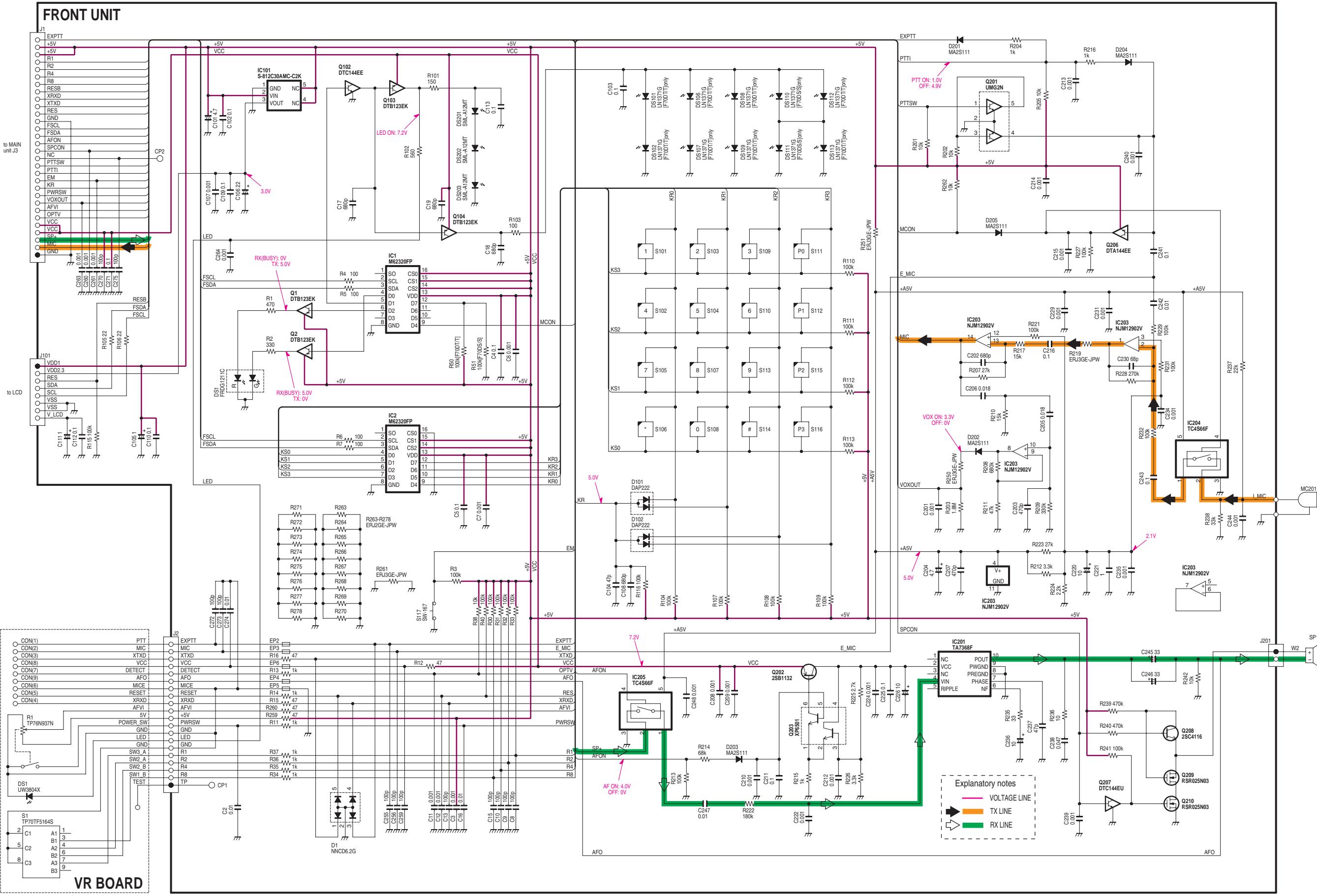


SECTION 10 BLOCK DIAGRAM

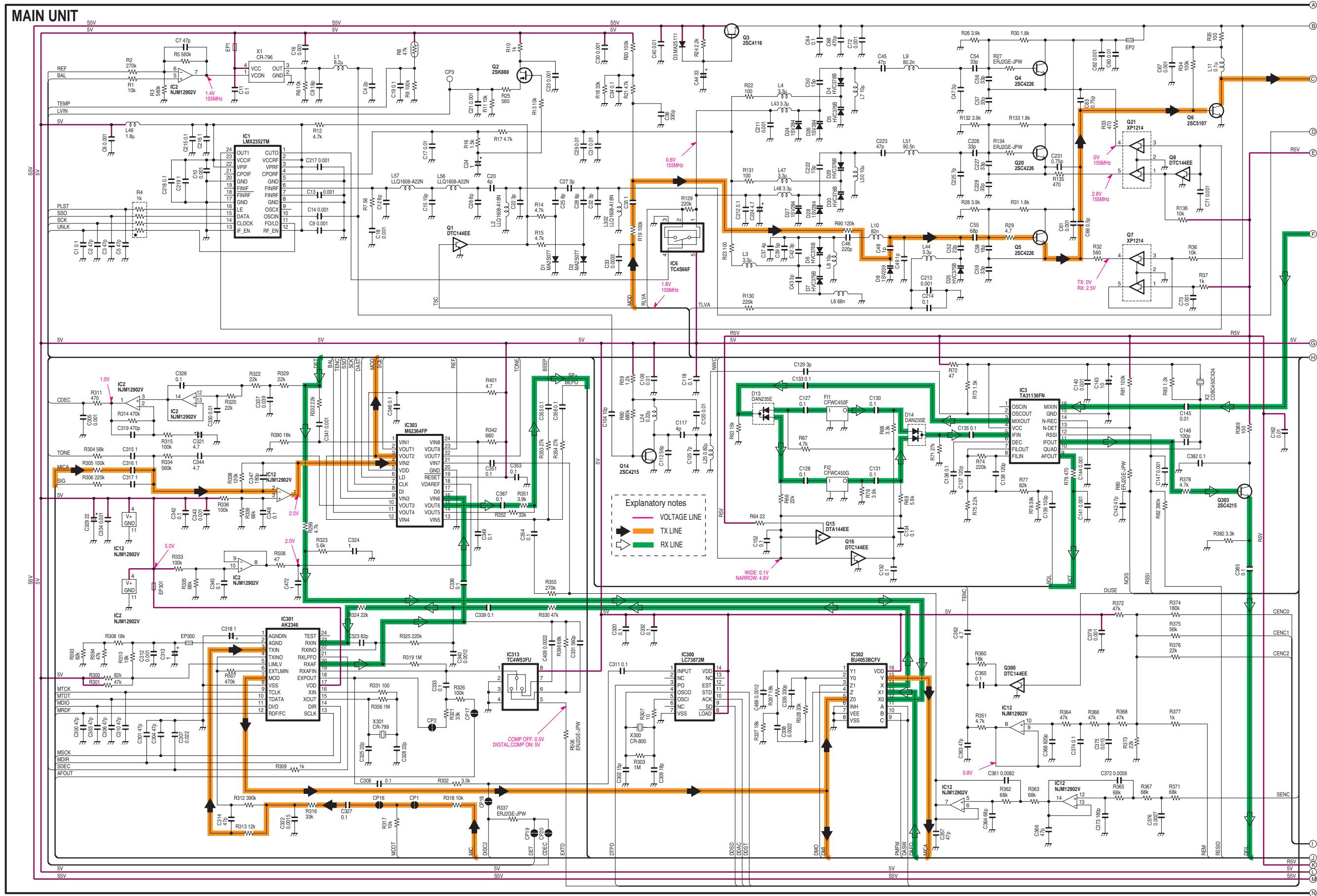


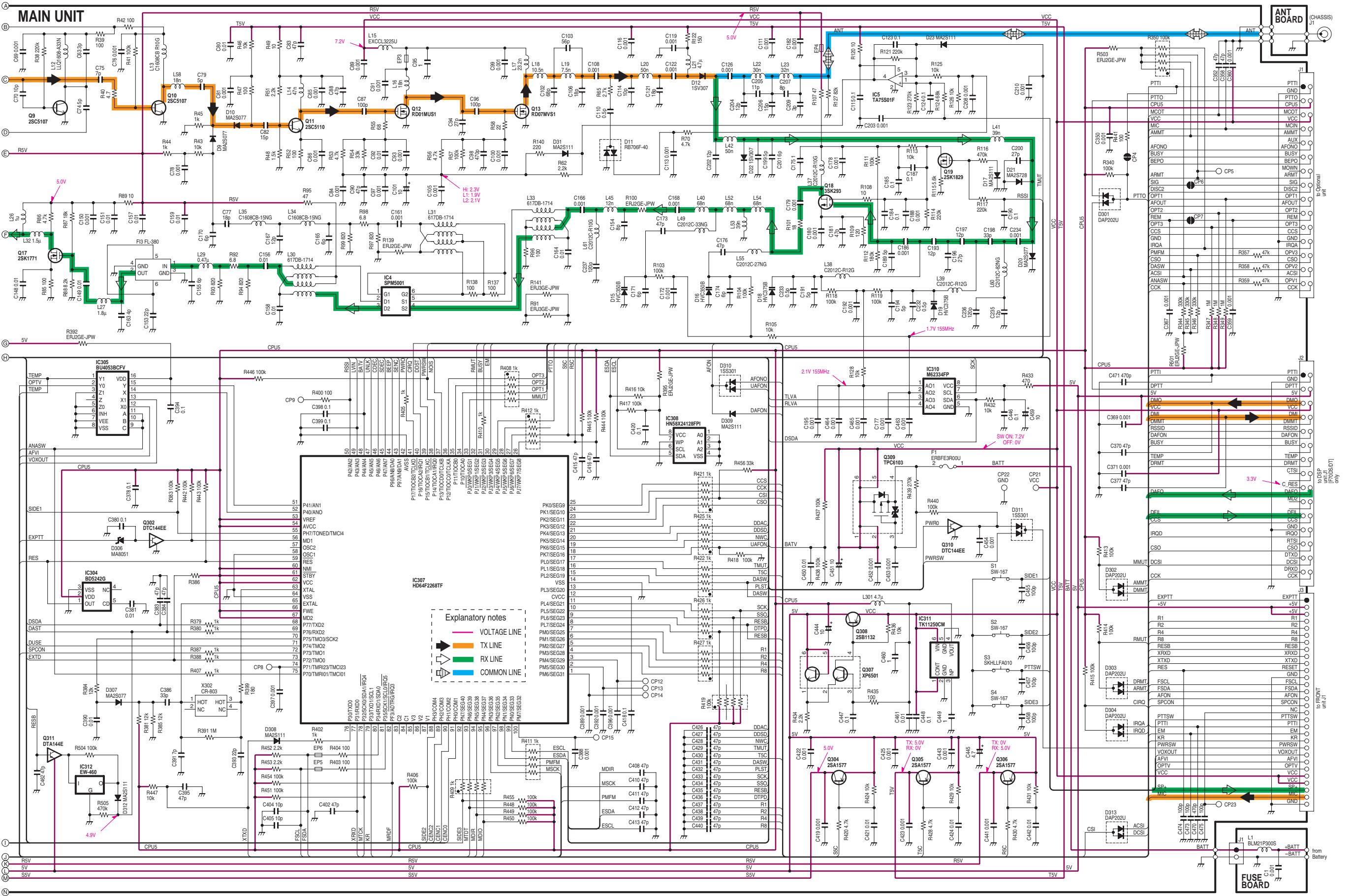
SECTION 11 VOLTAGE DIAGRAMS

11-1 FRONT UNIT

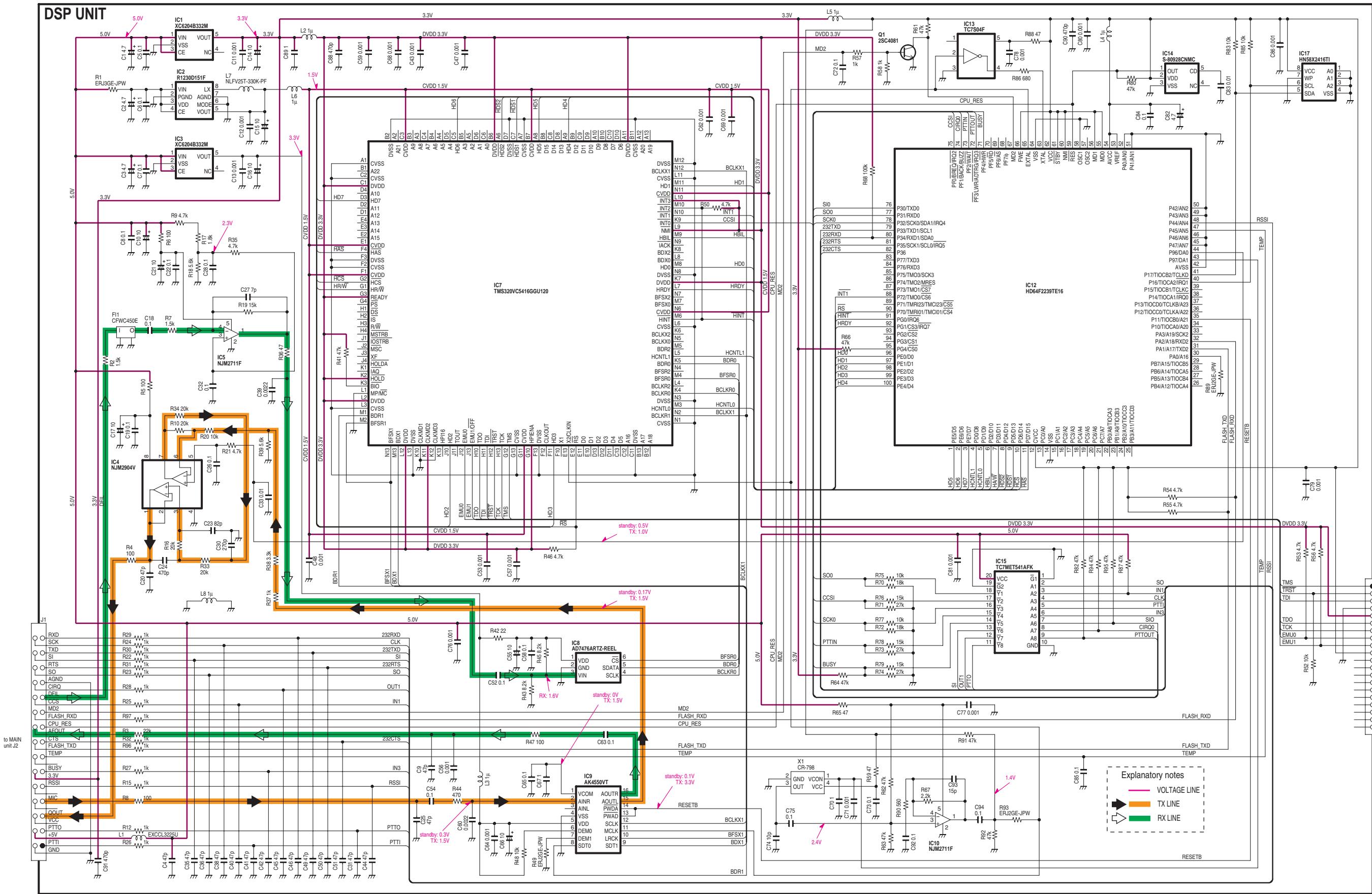


11-2 MAIN UNIT





11-3 DSP UNIT (IC-F70DT/DS only)



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