



SERVICE MANUAL

UHF TRANSCEIVERS

IC-F80DT/DS
IC-F80T/S

INTRODUCTION

This service manual describes the latest service information for the **IC-F80DT/DS** and **IC-F80T/S** UHF TRANSCEIVERS at the time of publication.

MODEL	VERSION	SYMBOL	APCO25	10-KEYPAD	
IC-F80DS	USA-02	[L]	Compatible	No	
	USA-03	[H]			
	USA-04	[L]	Not compatible		
	USA-05	[H]			
IC-F80S	USA-06	[L]	FM only		
	USA-07	[H]			
IC-F80DT	USA-02	[L]	Compatible	Yes	
	USA-03	[H]			
	USA-04	[L]	Not compatible		
	USA-05	[H]			
IC-F80T	USA-06	[L]	FM only		
	USA-07	[H]			

DANGER

NEVER connect the transceiver to an AC outlet or to a DC power supply that uses more than 7.2 V. Such a connection could cause a fire or electric hazard.

DO NOT expose the transceiver to rain, snow or any liquids.

DO NOT reverse the polarities of the power supply when connecting the transceiver.

DO NOT apply an RF signal of more than 20 dBm (100 mW) to the antenna connector. This could damage the transceiver's front end.

ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

1130010100 S.I.C LMX2352TM IC-F80DS Main unit 5 pieces
8810010121 Screw PH B0 M2x8 SUS SSBC IC-F80DS Chassis 10 pieces

Addresses are provided on the inside back cover for your convenience.



IC-F80DS/S

To upgrade quality, all electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

REPAIR NOTES

1. Make sure a problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated turning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 30 dB to 40 dB attenuator between the transceiver and a deviation meter or spectrum analyzer when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.

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TABLE OF CONTENTS

SECTION 1	SPECIFICATIONS	
SECTION 2	INSIDE VIEWS	
SECTION 3	DISASSEMBLY INSTRUCTIONS	
SECTION 4	CIRCUIT DESCRIPTION	
4 - 1	RECEIVE CIRCUITS.....	4 - 1
4 - 2	TRANSMITTER CIRCUITS.....	4 - 3
4 - 3	PLL CIRCUITS	4 - 4
4 - 4	POWER SUPPLY CIRCUITS.....	4 - 4
4 - 5	DIGITAL CIRCUIT (IC-F80DT/DS only).....	4 - 5
4 - 6	PORT ALLOCATIONS.....	4 - 5
SECTION 5	ADJUSTMENT PROCEDURES	
5 - 1	PREPARATION	5 - 1
5 - 2	SOFTWARE ADJUSTMENT.....	5 - 4
SECTION 6	PARTS LIST	
SECTION 7	MECHANICAL PARTS AND DISASSEMBLY	
SECTION 8	SEMICONDUCTOR INFORMATION	
SECTION 9	BOARD LAYOUTS	
9 - 1	FRONT UNIT.....	9 - 1
9 - 2	MAIN UNIT	9 - 3
9 - 3	FUSE BOARD	9 - 3
9 - 4	ANT BOARD	9 - 3
9 - 5	DSP UNIT (IC-F80DT/DS only).....	9 - 5
9 - 6	VR BOARD	9 - 5
SECTION 10	BLOCK DIAGRAM	
SECTION 11	VOLTAGE DIAGRAMS	
11 - 1	FRONT UNIT.....	11 - 1
11 - 2	MAIN UNIT	11 - 2
11 - 3	DSP UNIT (IC-F80DT/DS only).....	11 - 4

SECTION 1 SPECIFICATIONS

■ GENERAL

- Frequency coverage : 400–470 MHz
450–520 MHz
- Type of emission : 11K0F3E/8K10F1E (Narrow)
16K0F3E (Wide)
- Number of conventional channels : 256 channels (Max.)
- Antenna impedance : 50 Ω (Nominal)
- Operating temperature range : -22°F to 140°F
- Power supply requirement : Specified Icom's battery pack only
(Operable voltage; 7.2 V DC negative ground)
- Current drain (At 7.2 V DC ; approx.)

RECEIVING		TRANSMITTING (at 4 W)
Stand-by	Max.audio	2.4 A
150 mA	600 mA	
- Dimensions (Projections not included)
- Weight (Except antenna, battery pack) : 2 5/16 (W) x 5 31/32 (H) x 1 1/2 (D) in
9 5/32 oz (Approx.)

■ TRANSMITTER

- Output power (At 7.2 V DC) : 4 W
- Modulation : Variable reactance frequency modulation
- Maximum permissible deviation : ±2.5 kHz (Narrow)
±5.0 kHz (Wide)
- Frequency error : ±2.0 ppm
- Spurious emissions : 70 dB typ.
- Adjacent channel power : 60 dB (Narrow)
70 dB (Wide)
- Audio harmonic distortion : Less than 3%
- Limiting character of modulator : 60–100% of max. deviation
- FM hum and noise : 35 dB typ. (Narrow)
40 dB typ. (Wide)
- Audio frequency response : +2 dB to -8 dB of 6 dB/octave from 300 Hz to 2550 Hz (Narrow)
+2 dB to -8 dB of 6 dB/octave from 300 Hz to 3000 Hz (Wide)
- Microphone impedance : 600 Ω

■ RECEIVER

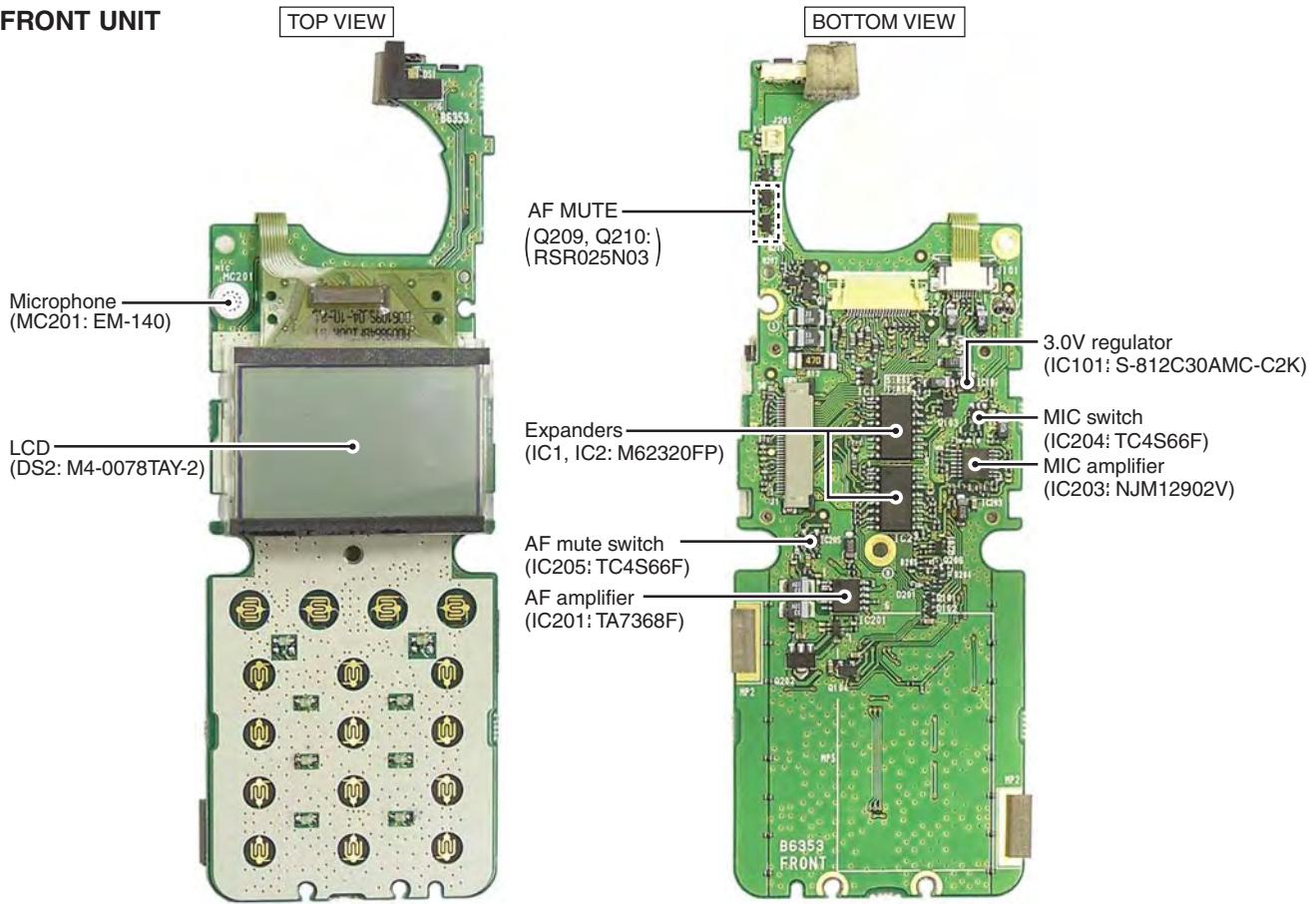
- Receive system : Double conversion superheterodyne system
- Intermediate frequencies : 1st IF; 46.35 MHz, 2nd IF; 450 kHz
- Sensitivity : 0.32 μV typ. at 12 dB SINAD
- Squelch sensitivity (At threshold) : 0.32 μV typ.
- Adjacent channel selectivity : 68 dB (Narrow)
73 dB (Wide)
- Spurious response : 73 dB
- Intermodulation rejection ratio : 65 dB (Narrow)
73 dB (Wide)
- Hum and Noise : 35 dB (Narrow)
40 dB (Wide)
- Audio output power : 0.35 W typ. at 5% distortion with an 8 Ω load
- Output impedance (Audio) : 8 Ω

Specifications are measured in accordance with EIA-152-C/204D, TIA-603.

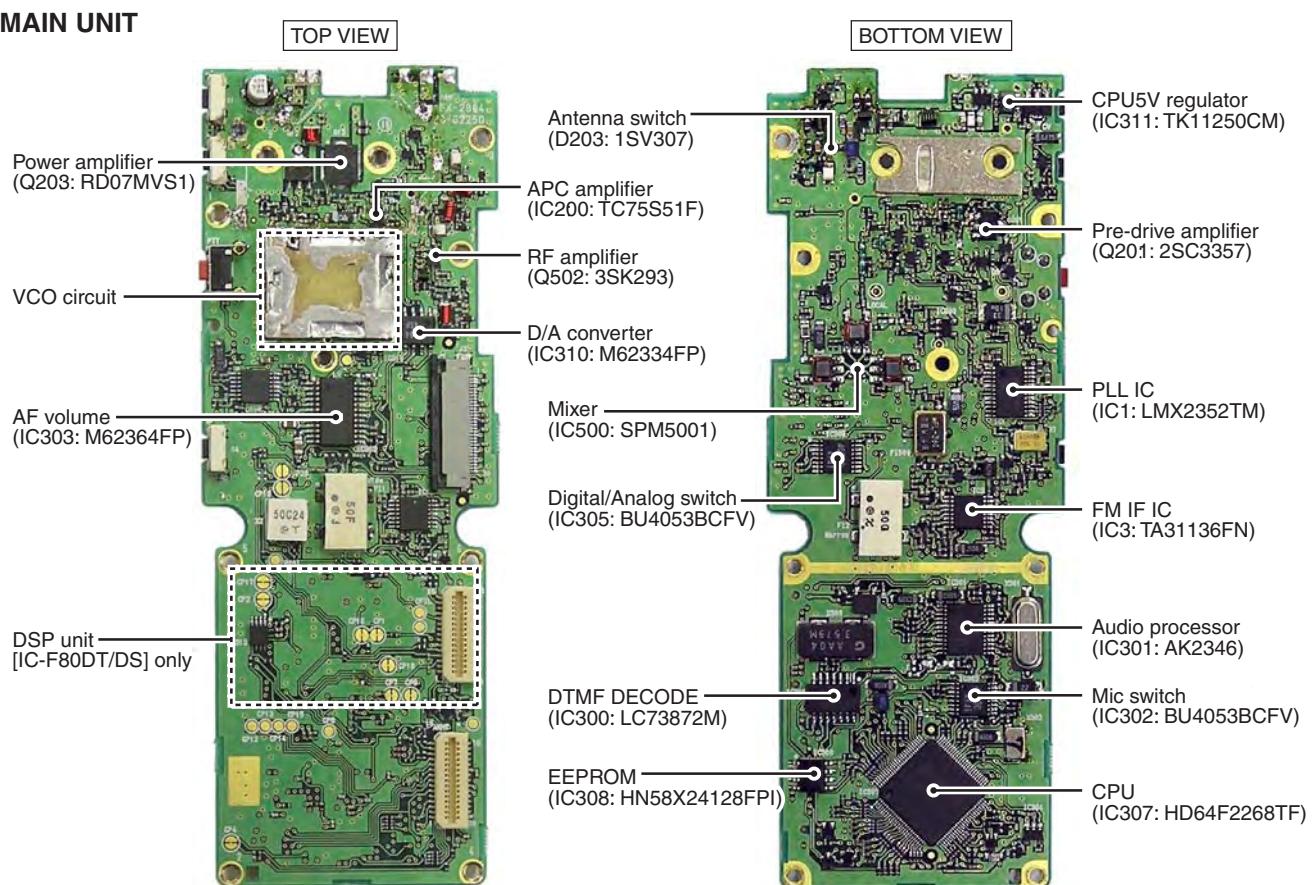
All stated specifications are subject to change without notice or obligation.

SECTION 2 INSIDE VIEWS

• FRONT UNIT



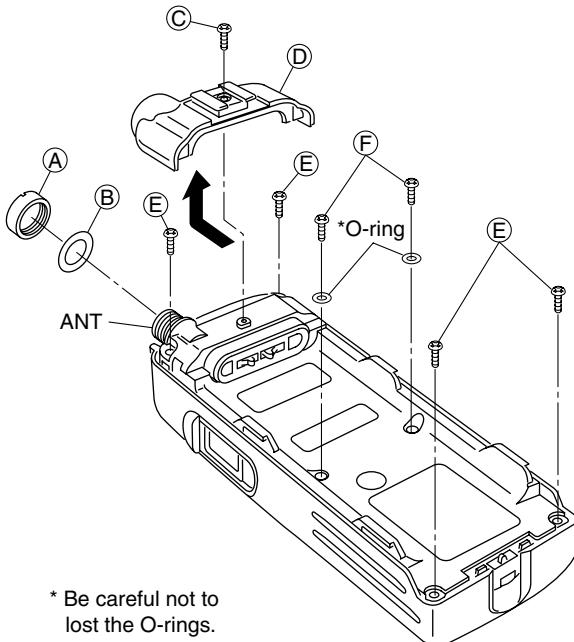
• MAIN UNIT



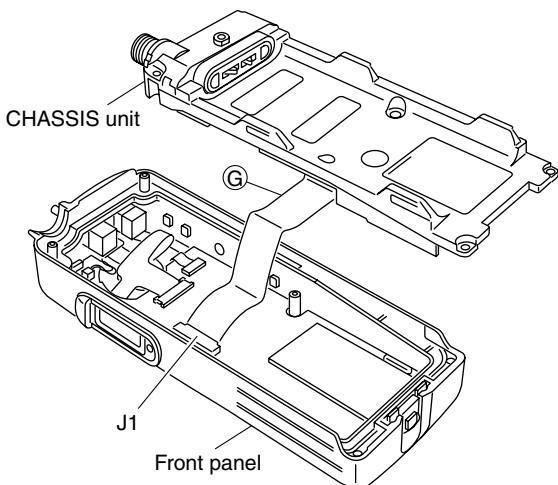
SECTION 3 DISASSEMBLY INSTRUCTIONS

• REMOVING THE CHASSIS UNIT

- ① Unscrew the ANT nut **(A)** and remove the ANT washer **(B)**.
- ② Unscrew the screw **(C)**, and remove the rear panel **(D)** in the direction of the arrow.
- ③ Unscrew 4 screws **(E)** and 2 screws **(F)**.

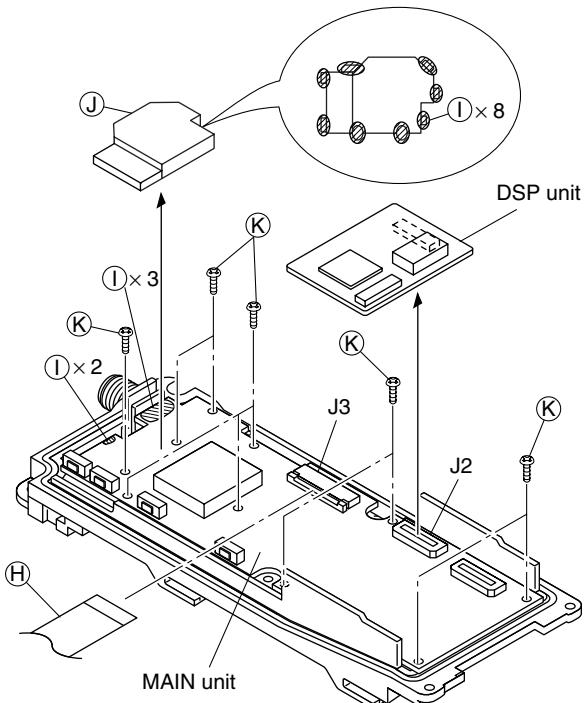


- ⑤ Disconnect the cable **(G)** from J1 and remove the CHASSIS unit from the front panel.



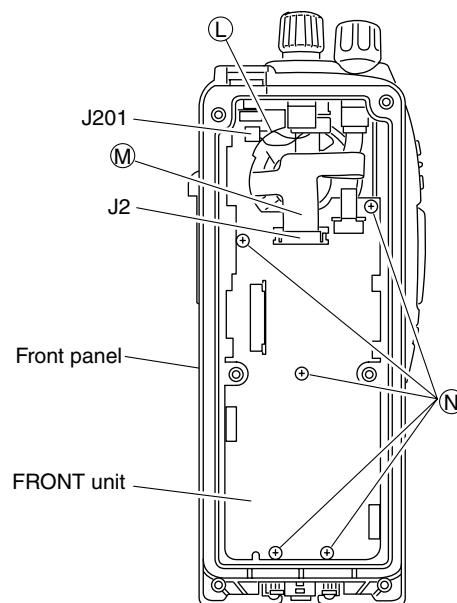
• REMOVING THE MAIN UNIT

- ① Disconnect the cable **(H)** from J3.
- ② Remove the DSP unit from J2.
- ③ Unsolder 13 points **(I)** and remove the shield plate **(J)**.
- ④ Unscrew 10 screws **(K)** and remove the MAIN unit from the CHASSIS.



• REMOVING THE FRONT UNIT

- ① Disconnect the speaker cable **(L)** from J201.
- ② Disconnect the cable **(M)** from J2.
- ③ Unscrew 5 screws **(N)** and remove the FRONT unit from the front panel.



SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT (MAIN UNIT)
The antenna switching circuit toggles the receive line and the transmit line. This circuit does not allow transmit signals to enter the receiver circuits.

Received signals from the antenna connector (CHASSIS UNIT; J1) are passed through a two-stage low-pass filter (LPF; L522, L523, C565–C569) and applied to the $\lambda/4$ type antenna switching circuit (D203, D510).

While receiving, no voltage is applied to D203 and D510. Thus, the receive line and the ground are disconnected and L520 and C564 function as an LPF which leads received signals to the RF circuits via the limiter (D509).

4-1-2 RF CIRCUITS (MAIN UNIT)

The RF circuits amplify received signals within the range of frequency coverage and filters off out-of-band signals.

The signals from the antenna switching circuit are passed through the two-stage tunable bandpass filters (BPF; D506, D507, L516, L517, C551, C552, C554–C556) to suppress unwanted signals. The filtered signals are amplified at the RF amplifier (Q502).

The amplified signals are passed through another two-stage tunable BPF (D502, D504, D505, L510, C520, C522, C523, C527, C530, C536, C538) to suppress unwanted signals again. The filtered signals are then applied to the 1st IF circuit.

4-1-3 1st IF CIRCUITS (MAIN UNIT)

The 1st IF circuits contain the 1st mixer, IF amplifier and the 1st IF filter circuits, and the 1st IF mixer converts the received signals into a fixed frequency of the 1st intermediate frequency (IF) signal. The converted 1st IF signal is filtered at the 1st IF filter, then amplified at the 1st IF amplifier.

The signals from the two-stage tunable BPF are converted into the 46.35 MHz 1st IF signal at the double-balanced type 1st mixer (IC500, L503, L504, L506) by being mixed with the 1st LO signal generated at the RX VCOs (Q600, D604, D605 for 400–434 MHz, Q601, D606, D607 for 435–470 MHz).

The 1st IF signal from the 1st mixer is passed through the crystal filter (FI500) to suppress unwanted signals, and then amplified at the 1st IF amplifier (Q500). The amplified 1st IF signal is applied to the FM IF IC (IC3, pin 16).

4-1-4 2nd IF AND FM DEMODULATOR CIRCUITS (MAIN UNIT)

The 1st IF signal is converted into the 2nd IF signal and demodulated at the detector section in the FM IF IC. The FM IF IC contains 2nd mixer, limiter amplifier, quadrature detector, etc. in its package.

The 1st IF signal from the 1st IF amplifier (Q500) is applied to the mixer section in FM IF IC (IC3, pin 16). The applied 1st IF signal is mixed with the 45.9 MHz 2nd LO signal generated by tripling the 15.3 MHz PLL reference frequency to be converted into the 450 kHz 2nd IF signal.

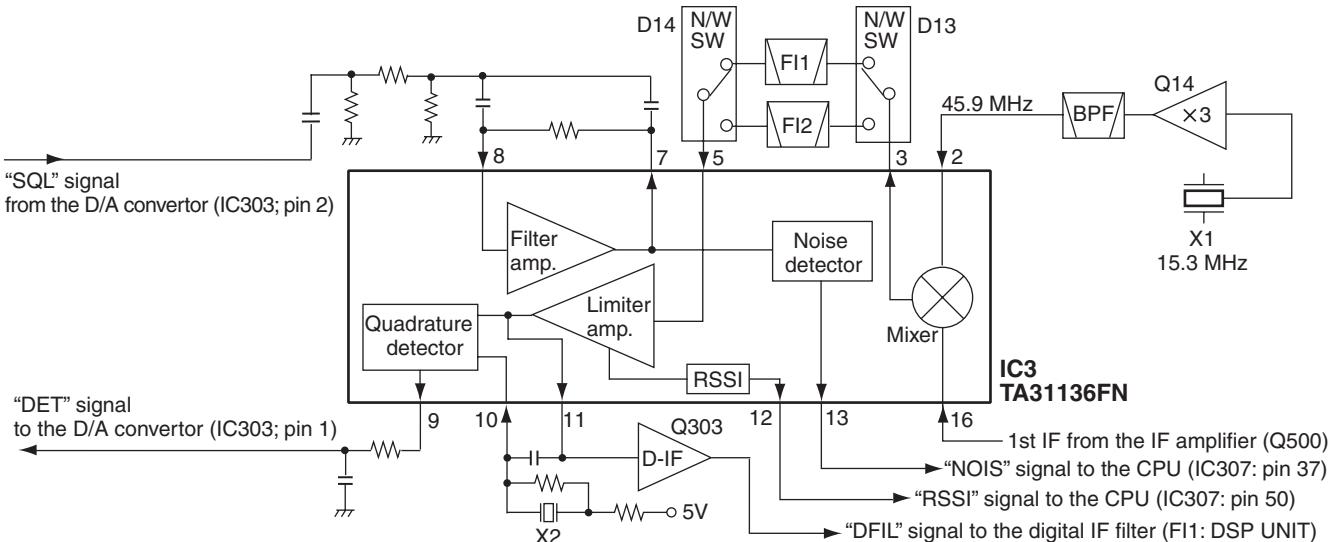
The 2nd IF signal from the mixer section is output from pin 3 and passed through the N/W switches (D13, D14) and a ceramic filter (FI1 or FI2) to suppress the heterodyne noise.

The N/W switches (D13, D14) toggle the receive mode wide and narrow according to “NWC” signal from the CPU (IC307, pin 19). FI1 is used for wide, and FI2 is used for narrow mode operation.

The filtered signal is applied to IC3 (pin 5) again, and amplified at the limiter amplifier section and demodulated by the quadrature detector.

The quadrature detector is a detection method which uses a ceramic discriminator (X2).

• 2ND IF AND DEMODULATOR CIRCUITS



The demodulated AF signals are output from pin 9, and applied to the AF circuits.

4-1-5 AF CIRCUITS (MAIN AND FRONT UNITS)

The demodulated AF signals from the FM IF IC are amplified and filtered at AF circuit. This transceiver employs the base band IC for audio signal processing for both transmit and receive. The base band IC is an audio processor and composed of pre-amplifier, compressor, expander, scrambler, etc. in its package.

The AF signals from FM IF IC (IC3, pin 9) are applied to the base band IC (IC301, pin 23) via the digital/analog switch (IC302, pins 12, 14).

The applied AF signals are amplified at the amplifier section and level adjusted at the volume control section, and then suppressed unwanted 3 kHz and higher audio signals at LPF section. The filtered AF signals are applied or bypassed the TX/RX HPF, de-scrambler, de-emphasis and expander sections in sequence, then applied to another volume controller.

The TX/RX HPF filters out 250 Hz and lower audio signals, and the de-emphasis obtains –6 dB/oct of audio characteristics. The expander expands the compressed audio signals and also noise reduction function is provided.

The AF signals are level adjusted at the volume controller and amplified at the amplifier section. The amplified AF signals are output from pin 20 and applied to the D/A converter (IC303, pin 16) to be adjusted its level. The level adjusted AF signals are then output from pin 15, and then applied to the FRONT UNIT via J3 (pin 28).

The level controlled AF signals from the MAIN UNIT are passed through the mute switch (FRONT UNIT; IC205, pins 1, 2) and applied to the AF power amplifier (FRONT UNIT; IC201, pin 4) to obtain 350 mW of AF output power. The power amplified AF signals are applied to the internal speaker (CHASSIS UNIT; SP1).

4-1-6 SQUELCH CIRCUITS (MAIN AND FRONT UNITS)

• NOISE SQUELCH

Noise squelch circuit mutes AF output signals when no RF signals are received. By detecting noise components in the demodulated AF signals, the squelch circuit switches the AF mute switch and AF power amplifier controller ON and OFF.

A portion of the demodulated AF signals from the FM IF IC (IC3, pin 9) are applied to the converter (IC303, pin 1) to be adjusted its level. The level controlled signals are output from pin 2 and applied to the active filter (IC3, pins 7, 8; R74, R75, R77, R78, C137–C139). The filtered signals are applied to the filter amplifier section to amplify the noise components only.

The amplified noise components are converted into the pulse-type signal at the noise detector section, and output from pin 13 as the "NOIS" signal and applied to the CPU (IC307, pin 37). Then the CPU outputs "AFON" signal from pin 18 according to the "NOIS" signal level to toggle the AF mute circuit (FRONT UNIT; IC205) and AF amplifier controller (FRONT UNIT; Q202, Q203) ON/OFF.

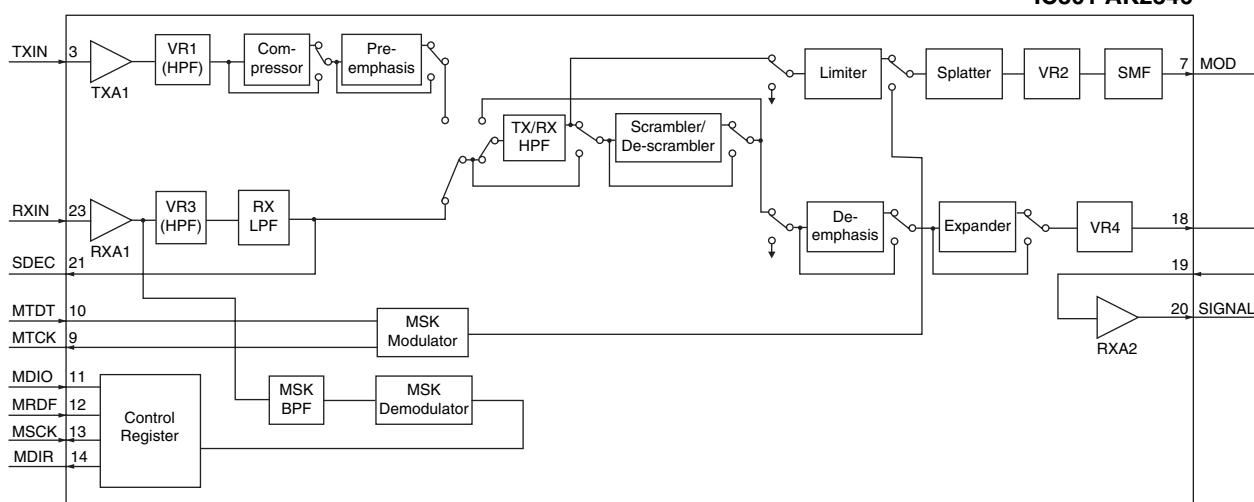
• CTCSS AND DTCS

The tone squelch circuit detects tone signals and opens the squelch only when receiving a signal containing a matched sub audible tone (CTCSS or DTCS). When the tone squelch is in use, and a signal with a mismatched or no sub audible tone is received, the tone squelch circuit mutes the AF signals even when the noise squelch is open.

A portion of the demodulated AF signals from the FM IF IC are passed through the LPF (IC2, pins 12, 14) to filter CTCSS/DTCS signal. The filtered signal is applied to the CPU (IC307, pin 46) after being amplified at the buffer amplifier (IC2, pins 1, 3).

The CPU compares the applied signal and the set CTCSS/DTCS, then output the "AFON" signal to the AF mute switch (FRONT UNIT; IC205) and AF amplifier controller (FRONT UNIT; Q202, Q203) control signal from pin 18.

• BASE BAND IC BLOCK DIAGRAM



4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT (FRONT AND MAIN UNITS)

The microphone amplifier circuit amplifies the audio signals from microphone within +6 dB/oct pre-emphasis characteristic. The microphone signals are processed in the base band IC which contains microphone amplifier, compressor, scrambler, limiter, splatter filter, etc. in its package.

The audio signals from the microphone (FRONT UNIT; MC201) are passed through the microphone mute switch (FRONT UNIT; IC204 pins 1, 2). The switched signals are amplified at the microphone amplifiers (FRONT UNIT; IC203, pins 1, 2, 13, 14) to obtain within +6 dB/oct pre-emphasis characteristics. The amplified signals are applied to the MAIN UNIT via J1 (pin 2).

The amplified MIC signals from the FRONT UNIT are applied to the base band IC (IC301, pin 3). The applied MIC signals are amplified at the amplifier section, and level adjusted at the volume control section. The level adjusted MIC signals are applied or bypassed the compressor, pre-emphasis, TX/RX HPF, scrambler, limiter and splatter sections in sequence, then applied to another volume controller.

The compressor compresses the MIC signals to provide high S/N ratio for receive side, and the pre-emphasis obtains +6 dB/oct audio characteristics. The TX/RX HPF filters out 250 Hz and lower audio signals, the limiter limits its level and the splatter filters out 3 kHz and higher audio signals.

The filtered MIC signals are level adjusted at another volume control section and amplified at the amplifier section, and then output from pin 7 via smoothing section (SMF).

4-2-2 MODULATION CIRCUIT (MAIN UNIT)

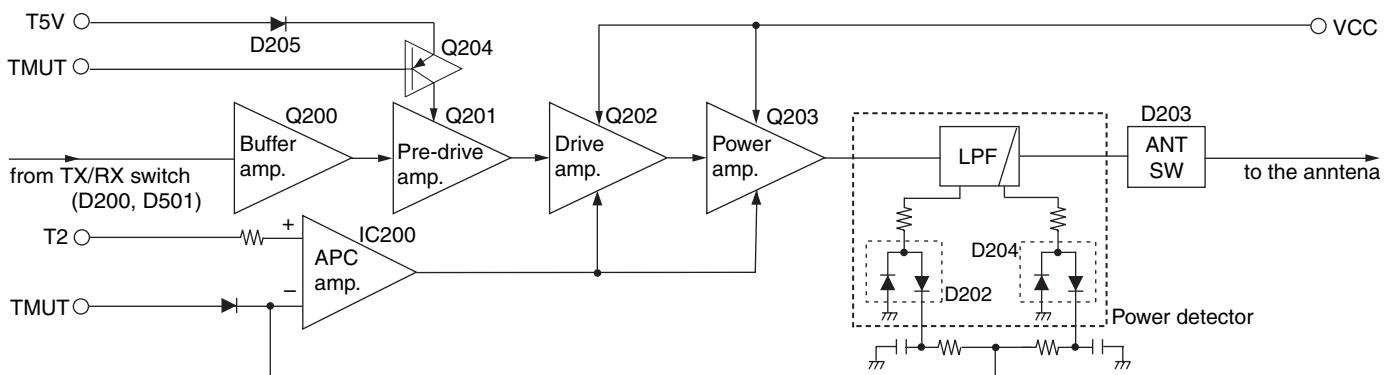
The modulation circuit modulates the VCO oscillating signal with the audio signals from the microphone.

MIC signals from the base band IC (IC301) are passed through the MIC switch (IC302, pins 4, 5), PM filter (C338, R327), FM/PM switch (IC302, pins 1, 15), and then applied to the AF mixer (IC12, pin 2) to be mixed with CTCSS/DTCS signals.

The mixed MIC signals are output from pin 1 and then applied to the D/A converter (IC303, pin 4) to be adjusted its level. The level adjusted AF signals are output from pin 3 and applied to the modulation circuit (D611) to modulate the VCO oscillating signal by changing the reactance of D611 at the TX VCO (Q602, D608, D609).

The CTCSS/DTCS signals are generated by the CPU (IC307)

• APC CIRCUIT



and output from pins 89–91 ("CENC0," "CENC1," "CENC2"). The CTCSS/DTCS signals are passed through 3 registers (R374–R376) to change its wave form. The wave form changed CTCSS/DTCS signals are then passed through the LPF (IC12, pins 8, 10) and applied to the converter (IC303, pin 9) to be adjusted its level, and output from pin 10.

The level adjusted CTCSS/DTCS signals are applied to the AF mixer (IC12, pin 2) to be mixed with MIC signals. The mixed CTCSS/DTCS signals are output from pin 1 and applied to the D/A converter (IC303, pin 4) to be adjusted its level again, then output from pin 3. The CTCSS/DTCS signals from the D/A converter are applied to the both of reference frequency oscillator (X1) and modulation circuit (D611) to modulate the reference frequency signal and VCO oscillating signal.

The modulated VCO output signal is amplified at the buffer amplifiers (Q605, Q606, Q609) and is then applied to the pre-drive amplifier (Q201) via the TX/RX switch (D200).

4-2-3 TRANSMIT AMPLIFIERS (MAIN UNIT)

The VCO output signal is amplified to transmit output power level by the transmit amplifiers .

The buffer-amplified signal from the TX/RX switch (D200) is applied to the pre-drive (Q201), drive (Q202), and power (Q203) amplifiers to be amplified to the transmit output power level. The power amplified transmit signal is passed through the power detector (D202, D204), antenna switch (D203), and two-stage LPFs (L522, L523, C565–C569), and then applied to the antenna connector (CHASSIS UNIT; J1).

4-2-4 APC CIRCUIT (MAIN UNIT)

The APC (Automatic Power Control) circuit stabilizes transmit output power and controls transmit output power High or Low.

The power detector circuits (D202, D204) detect the transmit output signal level and converts it into DC voltage.

The detected voltage is applied to the APC amplifier (IC200, pin 3). The "T2" signal from the D/A converter (IC310, pin 2), controlled by the CPU (IC307), is applied to the another input (pin 1) for reference, and the "T2" signal also controls transmit output power (4 W, 2 W or 1 W).

The output voltage from the APC amplifier controls the bias of the drive amplifier (Q202) and power amplifier (Q203) to control the output power by comparing the detected voltage and the reference voltage. Thus the APC circuit maintains a constant transmit output power.

4-3 PLL CIRCUITS

4-3-1 PLL CIRCUIT (MAIN UNIT)

The PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL circuit compares the phase of the divided VCO frequency with the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of the programmable divider.

The PLL circuit contains the two RX VCOs (Q600, D604, D605 for 400–434 MHz, Q601, D606, D607 for 435–470 MHz) and one TX VCO (Q602, D608, D609). The oscillated signal is amplified at the buffer amplifiers (Q605, Q606, Q608) and applied to the PLL IC (IC1, pin 6) after being passed through the LPF (L2, L3, C22, C25, C27, C28, C37).

The applied signal is divided at the prescaler and programmable divider section by the N-data ratio from the CPU (IC307). The divided signal is phase-compared with the deviated reference frequency at the phase detector. The phase difference is output from pin 4 as a pulse signal after being passed through the charge pump section. The output signal is passed through the loop filter (R16, R17, C17, C24, C29, C31) to converted into the DC voltage, and is then applied to the VCO circuits as the lock voltage.

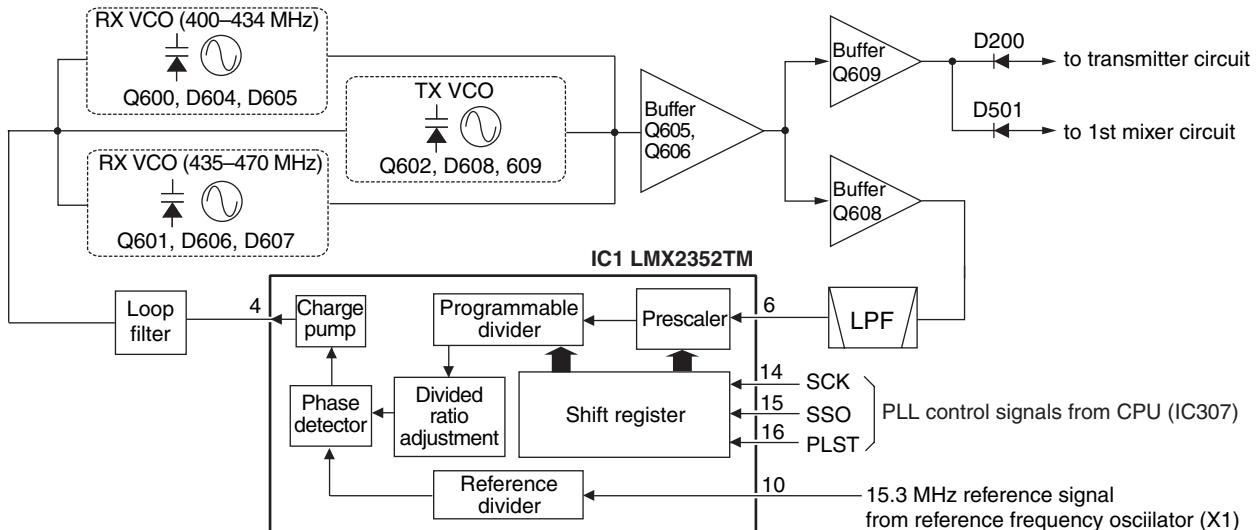
If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

4-3-2 VCO CIRCUITS (MAIN UNIT)

The VCO circuits contain separate two RX VCOs (Q600, D604, D605 for 400–434 MHz, Q601, D606, D607 for 435–470 MHz) and one TX VCO (Q602, D608, D609). The oscillated signal is amplified at the buffer amplifiers (Q605, Q606, Q609) and is then applied to the TX/RX switch (D200, D501). Then the receive 1st LO (RX) signal is applied to the 1st mixer (IC500, L503, L504, L506), and the transmit (TX) signal is applied to the buffer amplifier (Q200).

A portion of the signal from the buffer amplifier (Q605, Q606) is fed back to the PLL IC (IC1, pin 6) as the comparison signal via the buffer amplifier (Q608) and the LPF (L2, L3, C22, C25, C27, C28, C37).

• PLL CIRCUIT



4-4 POWER SUPPLY CIRCUITS

4-4-1 VOLTAGE LINES (MAIN UNIT)

LINE	DESCRIPTION
VCC	The voltage from the attached battery pack passed through the power switch (Q309).
CPU5V	Common 5 V for the CPU (IC307) converted from the VCC line at the CPU5V regulator (IC311).
5V	Common 5 V line converted from the VCC line at the +5V regulator (Q307, Q308).
T5V	5 V for the transmit circuits regulated from the 5V line by the T5V switch (Q305). The switch is controlled by the "T5C" signal from the CPU (IC307, pin 16).
S5V	5 V for the power save line regulated from the 5V line by the S5V switch (Q304). The switch is controlled by the "S5C" signal from the CPU (IC307, pin 27).
R5V	5 V for the receive circuits regulated from the 5V line by the R5V switch (Q306). The regulator is controlled by the "R5C" signal from the CPU (IC307, pin 26).

4-4-2 VOLTAGE LINES (DSP UNIT)

LINE	DESCRIPTION
DVDD3.3V	3.3 V for the CPU (IC12; DSP UNIT), DSP IC (IC7) and EEPROM (IC17) regulated from the 5V line by the +3VC regulator (IC1).
CVDD1.5V	1.5 V for the DSP IC (IC7) converted from the +5V line at the +1.5VA regulator (IC2).
+3VD	3.3 V for the A/D converter (IC8) and LINER CODEC IC (IC9) from the 5V line at the +3VD regulator (IC3).

4-5 DIGITAL CIRCUIT (IC-F80DT/DS only)

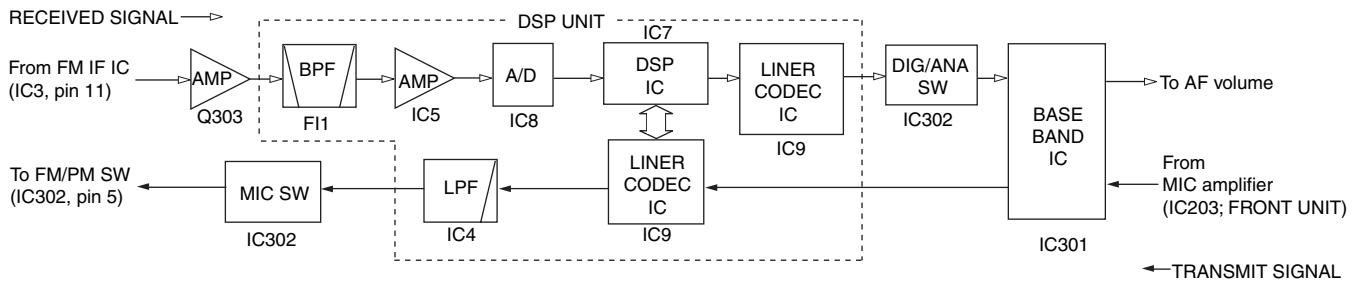
• WHILE RECEIVING

A portion of the 2nd IF signal from the limiter amplifier section in the FM IF IC (IC3) is output from pin 11 and is applied to the 2nd IF amplifier (Q303). The amplified 2nd IF signal is applied to the DSP UNIT via J2 (pin 11).

The 2nd IF signal from the MAIN UNIT is passed through the ceramic BPF (DSP UNIT; FI1) to suppress heterodyne noise, and amplified again at the digital IF amplifier (DSP UNIT; IC5, pin 4). The amplified 2nd IF signal is applied to the A/D converter (DSP UNIT; IC8, pin 3) to be converted into digital IF data, then applied to the DSP IC (DSP UNIT; IC7). The DSP IC converts the digital IF into the digital audio signal.

The digital audio signal from the DSP IC are converted into analog audio signals at the LINER CODEC IC (IC9) and output from pin 16. The audio signals from the LINER CODEC IC are applied to the MAIN UNIT via J1 (pin 22).

• DIGITAL MODE BLOCK DIAGRAM



4-6 PORT ALLOCATIONS

4-6-1 CPU (IC307)

Pin number	Port name	Description
4-7	R1, R2, R4, R8	Input ports for rotary selector (VR UNIT; S1).
10	SSO	Outputs serial data to the PLL IC (IC1, pin 15) and D/A converter (IC303, pin 8).
11	SCK	Outputs clock signal to the PLL IC (IC1 pin 14) and D/A converter (IC303, pin 7), etc.
13	PLST	Outputs strobe signals to the PLL IC (IC1, pin 16).
15	DASW	Outputs control signal to the digital/analog switch (IC302). Low: While analog mode is selected.
16	TXC	Outputs the T5V switch (Q305) control signal. Low: During transmit.
17	TMUT	• Outputs the APC amplifier (IC200) control signal. • Outputs the TX switch (Q204, D205) control signal. Low: During receive.
18	AFON	Outputs control signal for AF mute circuit (FRONT UNIT; IC205) and AF power amplifier (FRONT UNIT; IC201). High: AF amplifier (IC201) is activated.
19	NWC	Outputs wide/narrow switch (D13, D14) control signal. High: When narrow mode is selected.

The audio signals from the DSP UNIT are applied to the base band IC (MAIN UNIT; IC301, pin 20) after being passed through the digital/analog switch (MAIN UNIT; IC302).

• WHILE TRANSMITTING

The microphone signals from the base band IC (IC301, pin 7) are applied to the DSP UNIT via J2 (pin 4).

The microphone signals from the MAIN UNIT are applied to the LINER CODEC IC (DSP UNIT; IC9, pin 2) to convert into the digital audio signal.

The converted digital audio signal is processed by the DSP IC (DSP UNIT; IC7), and applied to the LINER CODEC IC (DSP UNIT; IC9) again. The signal from the LINER CODEC IC (IC9, pin 15) is passed through the LPFs (DSP UNIT; IC4, pins 3, 4, 5, 7) and applied to the MAIN UNIT via J1, and then passed through the microphone switch (MAIN UNIT; IC302, pins 3, 4), FM filter (R328, C335), FM/PM switch (IC302, pins 2, 15).

Pin number	Port name	Description
20	DDSD	Input port for serial data from the DTMF decoder IC (IC300, pin 9).
21	DDAC	Outputs clock signals to the DTMF decoder IC (IC300, pin 10).
26	R5C	Outputs R5V switch (Q306) control signal. High:While receiving.
27	S5C	Outputs S5V switch (Q304) control signal. High:In power save mode..
29	PTTO	Input port for optional unit. Low: Switch ON.
30	EM	Input port for the emergency switch (FRONT UNIT; S117). Low: While emergency switch is pushed.
32	RMUT	Input port for the AF mute signal from the optional unit via J1 or J2. Low: While RX audio is muted.
33	MMUT	Input port for the microphone mute signal from the optional unit via J1 or J2. Low: While microphone audio is muted.
34-36	OPT1- OPT3	I/O ports for the connected optional unit to J1.
37	NOIS	Input port for the noise signal from the FM IF IC (IC3, pin 13).

4-6-1 CPU (continued)

Pin number	Port name	Description
38	PWRSW	Input port for the [VOL] control (VR UNIT; R1). Low: While power is ON.
39	DDST	Input port for the decodedDTMF signals from the DTMF decoder IC (IC300, pin 11).
40	CIRQ	Inputs offering signal from the optional unit and DSP unit. Low: Offering signal is output.
41	PWRO	Outputs control signal for the power switch circuit (Q309, Q310). High: Power ON.
43	SENC	Outputs single tone encode signal.
44	BEEP	Outputs beep audio signals.
45	SDEC	Input port for single tone decode signal from the base band IC (IC301, pin 1).
46	CDEC	Input port for CTCSS/DTCS signal from the LPF (IC12, pin 7).
47	ULCK	Input port for the PLL unlock signal. Low: The PLL circuit is unlocked.
48	BATV	Input port for the connected battery pack for the low battery voltage detection. Low: The battery voltage is low.
49	LVIN	Input port for the PLL lock voltage.
50	RSSI	Input port for the "RSSI" signal from the FM IF IC (IC3, pin 12).
51	TEMP/OPTV	<ul style="list-style-type: none"> • Input port for the transceiver's internal temperature detecting signal. High: Internal temperature is high. • Input port for the optional unit detecting signal. High: While connecting optional unit to the multiconnector.
55	SIDE1	Input port for [UP] switch (MAIN UNIT; S1). Low: While [UP] switch is pushed.
68	DAST	Outputs strobe signals to the D/A converter (IC303, pin 6).
69	DSDA	I/O port for data signal to the D/A converter (IC310, pin 6).
72	SPCON	Outputs "SPCON" signal. Low: Audio output.
78	MTCK	Input port for transmitting MSK clock signal from the base band IC (IC301, pin 9).
79	KR	Input port for key matrix. Low: While any of key on the 10-keypad (including [P0]–[P3]) is pushed.
80	FSDA	I/O port for the serial data signal for the expander (FRONT UNIT; IC2).
81	FSCL	Outputs clock signal to the expander (FRONT UNIT; IC2).
88	SIDE2	Input port for [DOWN] switch (MAIN UNIT; S2). Low: While [DOWN] switch is pushed.
89–91	CENC0–CENC2	Output the CTCSS/DTCS signals.

Pin number	Port name	Description
92	SIDE3	Input port for [MONITOR] switch (MAIN UNIT; S4). Low: While [MONITOR] switch is pushed.
93	MTDT	Outputs the MSK data to the base band IC (IC301, pin 10).
94	MDIR	Outputs serial data control signal to the base band IC (IC301, pin 14).
95	MDIO	I/O port for the serial data signals from/to the base band IC (IC301, pin 11).
96	MSCK	Outputs clock signal for the base band IC (IC301, pin 13).
97	PMFM	Outputs the FM/PM switch (IC302, pin 11) control signal. High: While PM is selected.
98	ESDA	I/O port for data signals from/to the EEPROM (IC308, pin 5).
99	ESCL	Outputs clock signal to the EEPROM (IC308, pin 6).
100	CODE8	Output port for "CODE8" signal.

4-6-2 D/A CONVERTER (MAIN UNIT; IC303)

Pin number	Port name	Description
2	SQL	Outputs AF signals to the squelch circuit (IC3, pin 8).
3	MOD	Outputs modulation signals to the modulation circuit (D8).
10	TENC	Outputs CTCSS/DTCS signals.
11	BAL	Outputs deviation balance control signal.
14	BEPV	Outputs beep audio signals to the speaker via the AF amplifier (FRONT UNIT; IC201).
15	SIGNAL	Outputs AF signals to the speaker via the AF amplifiers (FRONT UNIT; IC201).
22	TONE	Outputs single tone signal.
23	REF	Outputs reference oscillator control signal.

4-6-3 D/A CONVERTER (MAIN UNIT; IC310)

Pin number	Port name	Description
1	T1	Outputs the bandpass filters (D18, D19) tuning signal.
2	T2	<ul style="list-style-type: none"> • While receiving: Outputs the bandpass filters (D15, D16) tuning signal. • While transmitting: Outputs the TX power control signal which selects TX output power of HIGH or LOW. The output signal is applied to the ALC amplifier (IC5, pin 1).
3	TXLVA	Outputs TX VCO lock voltage.
4	RXLVA	Outputs RX VCO lock voltage.

SECTION 5 ADJUSTMENT PROCEDURES

5-1 PREPARATION

When adjusting IC-F80DT/DS/D/S, the optional CS-F70/F1700 ADJ ADJUSTMENT SOFTWARE (Rev. 1.1 or later), OPC-966 JIG CABLE (modified OPC-966 CLONING CABLE; see illustration page 5-2) are required.

■ REQUIRED TEST EQUIPMENTS

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 7.2 V DC Current capacity : 3 A or more	Audio generator	Frequency range : 300–3000 Hz Measuring range : 1–500 mV
FM deviation meter	Frequency range : DC–600 MHz Measuring range : 0 to ±10 kHz	Attenuator	Power attenuation Capacity : 50 or 60 dB : 10 W
Frequency counter	Frequency range : 0.1–600 MHz Frequency accuracy : ±1 ppm or better Sensitivity : 100 mV or better	Standard signal generator (SSG)	Frequency range : 0.1–600 MHz Output level : 0.1 µV to 32 mV (-127 to -17 dBm)
Digital multimeter	Input impedance : 10 MΩ/V DC or more	AC millivoltmeter	Measuring range : 10 mV to 10 V
RF power meter	Measuring range : 1–10 W Frequency range : 100–600 MHz Impedance : 50 Ω SWR : Better than 1.2 : 1	Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–20 V
		External speaker	Input impedance Capacity : 8 Ω : 1 W or more

■ SYSTEM REQUIREMENTS

- Microsoft® Windows® 98/98SE/Me/2000/XP
- RS-232C serial port (D-sub 9 pin)

■ ADJUSTMENT SOFTWARE INSTALLATION

- Quit all applications when Windows is running.
- Insert the CD into the appropriate CD drive.
- Double-click the “Setup.exe” contained in the ‘CS-F70/F1700 ADJ’ folder in the CD drive.
- The “Welcome to the InstallShield Wizard for CS-F70/F1700 ADJ” will appear. Click [Next>].
- The “Choose Destination Location” will appear. Then click [Next>] to install the software to the destination folder. (e.g. C:\Program Files\Icom\CS-F70/F1700 ADJ)
- After the installation is completed, the “InstallShield Wizard Complete” will appear. Then click [Finish].
- Eject the CD.
- Program group ‘CS-F70/F1700 ADJ’ appears in the ‘Programs’ folder of the start menu, and ‘CS-F70/F1700 ADJ’ icon appears on the desk top screen.

■ BEFORE STARTING SOFTWARE ADJUSTMENT

Clone the adjustment frequencies into the transceiver, and set the configuration using with the CS-F70/F1700 CLONING SOFTWARE before starting the software adjustment. Otherwise, the transceiver can not start software adjustment.

CAUTION!: **BACK UP** the originally programmed memory data in the transceiver before programming the adjustment frequencies.

When program the adjustment frequencies into the transceiver, the transceiver’s memory data will be overwritten and lose original memory data at the same time.

Microsoft and Windows are registered trademarks of Microsoft Corporation in the U.S.A. and other countries.

■ STARTING SOFTWARE ADJUSTMENT

- Connect the transceiver and PC with OPC-966 JIG CABLE.
- Turn the transceiver power ON.
- Boot up Windows, and click the program group ‘CS-F70/F1700 ADJ’ in the ‘Programs’ folder of the [Start] menu, then CS-F70/F1700 ADJ’s window appears.
- Click ‘Connect’ on the CS-F70/F1700 ADJ’s window, then appears transceiver’s up-to-date condition.
- Set or modify adjustment data as desired.

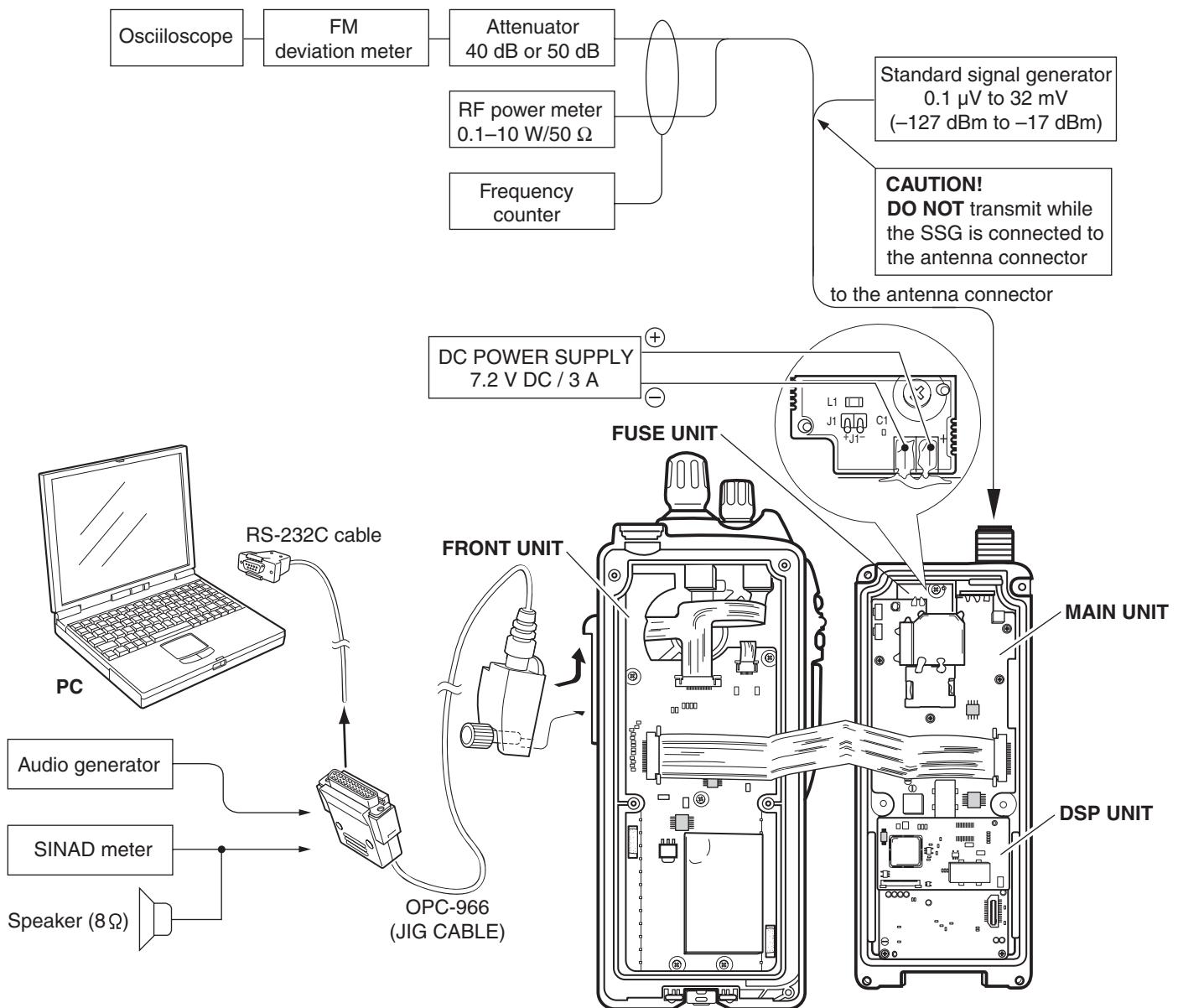
• ADJUSTMENT FREQUENCY LIST

CH	FREQUENCY (MHz)		ADJUSTMENT ITEM
	[L]	[H]	
1	400.000	450.000	TX power : Low1 Mode : Narrow
2	435.000	485.000	TX power : Low1 Mode : Narrow
3	470.000	520.000	TX power : Low1 Mode : Narrow
4	435.000	485.000	TX power : Low1 Mode : Wide
5	400.000	450.000	TX power : Low1 Mode : Wide
6	435.000	485.000	TX power : High Mode : Wide
7	435.000	485.000	TX power : Low2 Mode : Wide
8	470.000	520.000	TX power : Low1 Mode : Wide
9*	435.000	485.000	TX power : Low1 Mode : Digital Preamble Length [†] : 270
10*	400.000	450.000	TX power : Low1 Mode : Digital Preamble Length [†] : 270
11*	470.000	520.000	TX power : Low1 Mode : Digital Preamble Length [†] : 270
12	435.000	485.000	TX power : Low1 Mode : Wide CTCSS : 151.4 Hz DTCS : 007

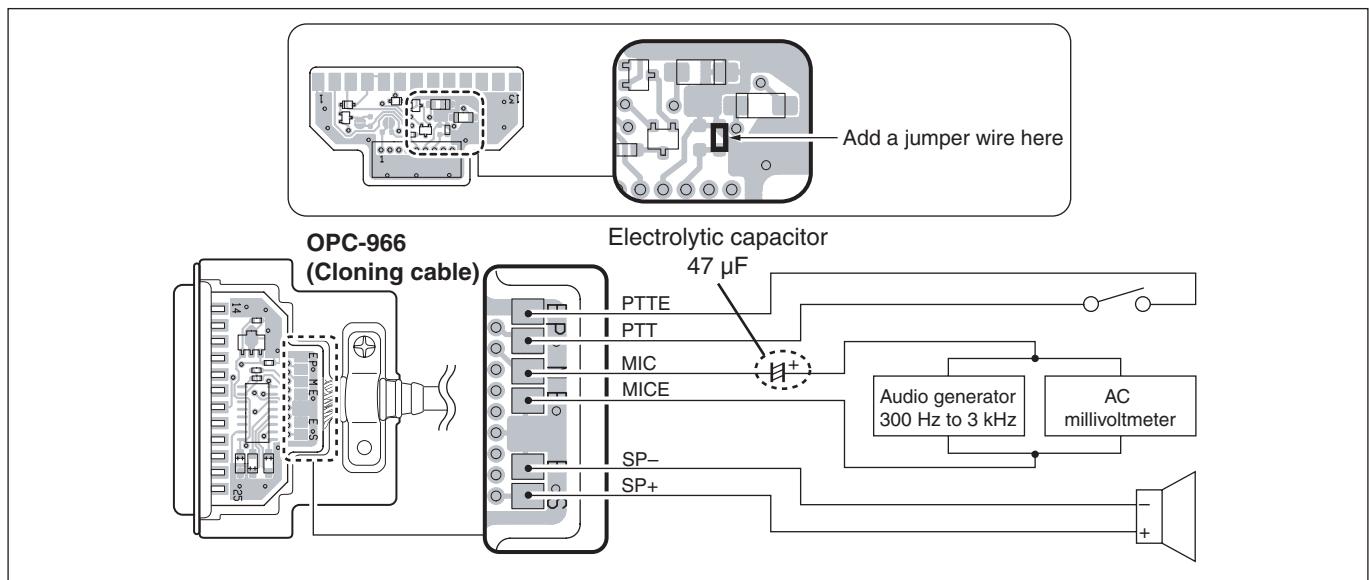
[†]; [USA-02], [USA-03], [USA-21], [USA-22] only

*; IC-F80DT/DS only

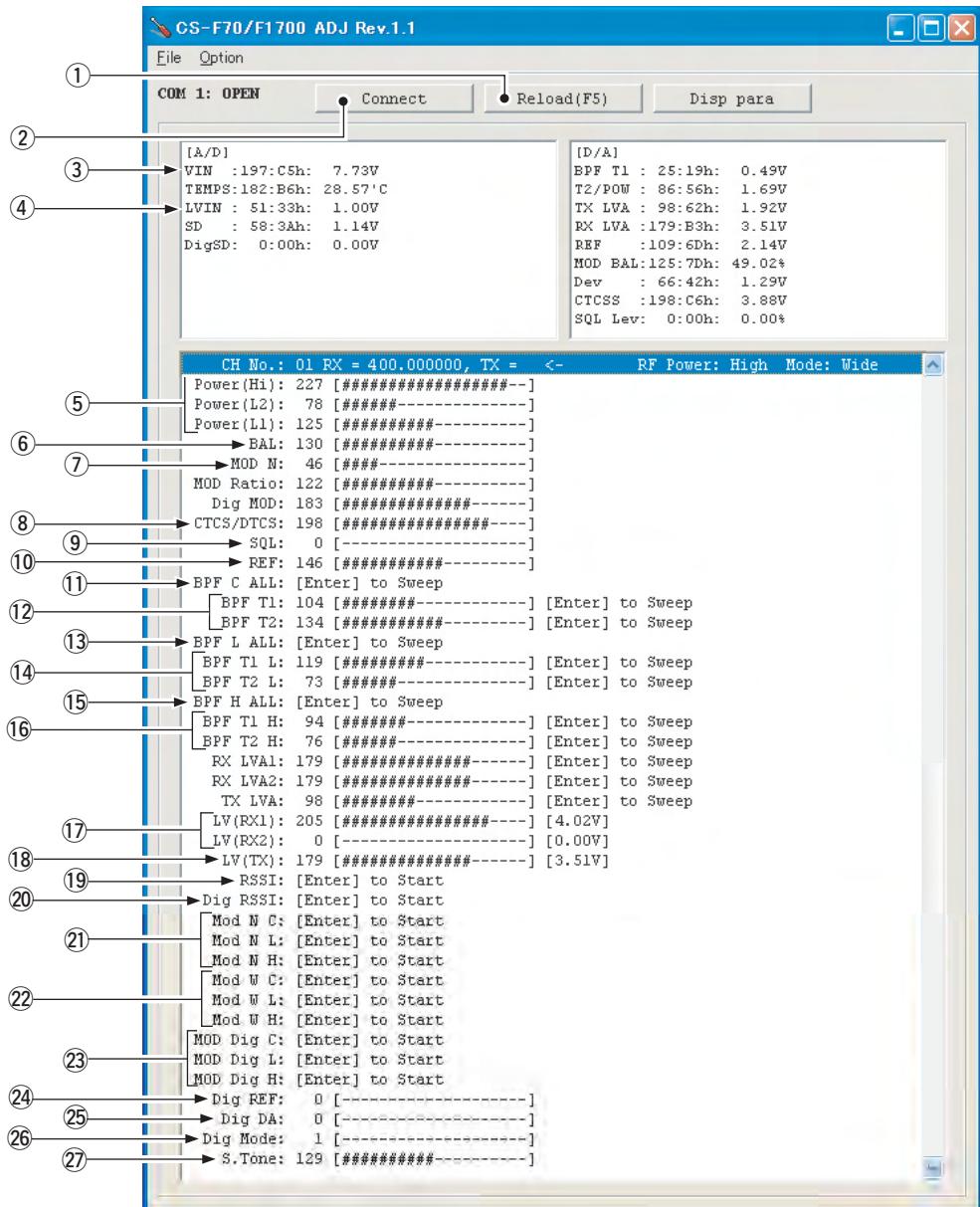
• CONNECTION



• JIG cable



• PC SCREEN EXAMPLE



NOTE: The above values for settings are example only.

Each transceiver has its own specific values for each setting.

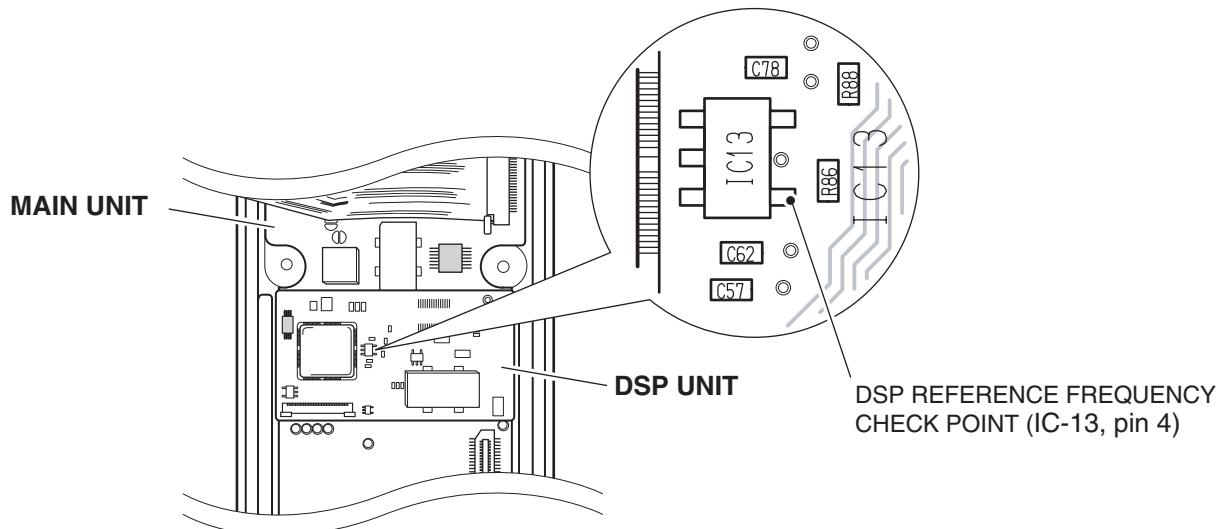
- | | | |
|-------------------------------------|--|-----------------------------|
| ①: Reload adjustment data | ⑩: Reference frequency | ⑯: S-meter (FM) |
| ②: Transceiver's connection state | ⑪: Receive sensitivity for center (automatic) | ⑰: S-meter (digital) |
| ③: Connected DC voltage measurement | ⑫: Receive sensitivity for center (manual) | ㉑: Deviation (narrow) |
| ④: PLL lock voltage measurement | ⑬: Receive sensitivity for low edge (automatic) | ㉒: Deviation (wide) |
| ⑤: RF output power | ⑭: Receive sensitivity for low edge (manual) | ㉓: Deviation (digital) |
| ⑥: FM modulation balance | ⑮: Receive sensitivity for high edge (automatic) | ㉔: DSP reference frequency |
| ⑦: FM modulation preset | ⑯: Receive sensitivity for high edge (manual) | ㉕: Base band center voltage |
| ⑧: CTCSS/DTCS deviation | ⑰: PLL lock voltage preset for RX (automatic) | ㉖: Digital mode |
| ⑨: Squelch level | ㉗: PLL lock voltage preset for TX (automatic) | ㉘: 2/5 TONE, DTMF deviation |

5-2 SOFT WARE ADJUSTMENT

Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard

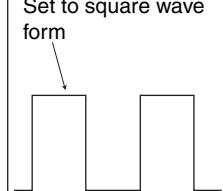
ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE
			UNIT	OPERATION	
PLL LOCK VOLTAGE	1	• Operating CH. : CH 1 • Receiving	PC screen	Click [Reload (F5)] button, then check the "LVIN" item on the CS-F70/F1700 ADJ's screen.	0.75–1.45 V (Verify)
	2	• Operating CH. : CH 2 • Receiving			0.55–1.35 V (Verify)
	3	• Operating CH. : CH 3 • Connect an RF power meter or 50 Ω dummy load to the antenna connector. • Transmitting			0.55–1.15 V (Verify)
REFERENCE FREQUENCY [REF]		• Operating CH. : CH 3 • Connect an RF power meter or 50 Ω dummy load to the antenna connector. • Transmitting	Top panel	Loosely couple a frequency counter to the antenna connector.	470.000000 MHz [L] 520.000000 MHz [H] ±100 Hz
DSP REFERENCE FREQUENCY* [Dig REF]		• Operating CH. : CH 8 • Receiving	DSP unit	Connect a frequency counter to the pin 4 of IC13 on the DSP unit through a 1000 pF capacitor. (see the illust below)	12.288000 MHz
BASE BAND CENTER VOLTAGE* [Dig DA]		• Operating CH. : CH 8 • Receiving	PC screen	Set the "Dig DA" item to 70.	

*; IC-F80DT/DS only



SOFTWARE ADJUSTMENT (Continued)

Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE
			UNIT	OPERATION	
OUTPUT POWER [Power (Hi)]	1	• Operating CH. : CH 6 • Transmitting	Top panel	Connect an RF power meter to the antenna connector.	4.0 W
[Power (L2)]	2	• Operating CH. : CH 7 • Transmitting			2.0 W
[Power (L1)]	3	• Operating CH. : CH 2 • Transmitting			1.0 W
MODULATION BALANCE [BAL]	1	• Operating CH. : CH 4 • Preset [MOD N] : 30 • No audio applied to the JIG cable. • Set an FM deviation meter as; HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P-P)/2 • Push [P0] while transmitting.	Top panel	Connect an FM deviation meter with an oscilloscope to the antenna connector through an attenuator.	 Set to square wave form
FM DEVIATION (NARROW) [MOD N C]	1	• Operating CH. : CH 2 • Connect an audio generator to the JIG cable and set as; : 1.0 kHz/150 mV rms • Set an FM deviation meter as; HPF : OFF LPF : 20 kHz De- emphasis : OFF Detector : (P-P)/2 • Transmitting			
(NARROW) [MOD N L]	2	• Operating CH. : CH 1 • Transmitting			
(NARROW) [MOD N H]	3	• Operating CH. : CH 3 • Transmitting			
(WIDE) [MOD W C]	4	• Operating CH. : CH 4 • Transmitting			
(WIDE) [MOD W L]	5	• Operating CH. : CH 5 • Transmitting			
(WIDE) [MOD W H]	6	• Operating CH. : CH 8 • Transmitting			

SOFTWARE ADJUSTMENT (Continued)

Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE
			UNIT	OPERATION	
DIGITAL DEVIATION* [MOD Dig C]	1	• Preset [Dig Mode] : 7	Top panel	Connect an FM deviation meter to the antenna connector through an attenuator.	± 2.80 to ± 2.90 kHz
	2	• Operating CH. : CH 9 • Set an FM deviation meter as; HPF : OFF LPF : 20 kHz De- emphasis : OFF Detector : (P-P)/2 • Transmitting			
	3	• Operating CH. : CH 10 • Transmitting			
	4	• Operating CH. : CH 11 • Transmitting			
DIGITAL DEVIATION* [MOD Dig C]	1	• Preset [Dig Mode] : 6	Top panel	Connect an FM deviation meter to the antenna connector through an attenuator.	± 0.91 to ± 1.01 kHz (Verify)
	2	• Operating CH. : CH 9 • Transmitting			
	3	• Operating CH. : CH 10 • Transmitting			
	4	• Operating CH. : CH 11 • Transmitting			
CTCSS/DTCS DEVIATION [CTCSS/DTCS]	1	• Operating CH. : CH 12 • No audio applied to the JIG cable. • Set an FM deviation meter as; HPF : OFF LPF : 20 kHz De- emphasis : OFF Detector : (P-P)/2 • Transmitting	Top panel	Connect an FM deviation meter to the antenna connector through an attenuator.	± 0.60 to ± 0.70 kHz
2/5 TONE /DTMF DEVIATION [S.Tone]	1	• Operating CH. : CH 2 • No audio applied to the JIG cable. • Set an FM deviation meter as; HPF : OFF LPF : 20 kHz De- emphasis : OFF Detector : (P-P)/2 • Push [P3] while transmitting.	Top panel	Connect an FM deviation meter to the antenna connector through an attenuator.	± 1.50 kHz

*; [IC-F80DT/DS] only

SOFTWARE ADJUSTMENT (continued)

- Select an operation using [\uparrow / \downarrow] keys, then set specified value using [\leftarrow / \rightarrow] keys on the connected computer keyboard

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE
		UNIT	LOCATION	
RX SENSITIVITY [BPF T1], [BPF T2]	NOTE: Need to adjust "S-METER ADJUSTMENT" after "RX SENSITIVITY ADJUSTMENT" is adjusted. Otherwise, "S-METER ADJUSTMENT" will not be adjusted properly.			
	1 • Operating CH : CH 4 • Connect the SSG to the antenna connector and set as; Frequency : 435.000 MHz [L] 485.000 MHz [H] Level : +20 dB μ [†] (-87 dBm) Modulation : 1 kHz Deviation : \pm 3.0 kHz • Receiving	PC screen	Connect the SINAD meter with an 8 Ω load to the JIG cable.	Minimum distortion level
[BPF T1 L], [BPF T2 L]	2 • Operating CH : CH 5 Frequency : 400.000 MHz [L] 450.000 MHz [H] • Receiving			
[BPF T1 H], [BPF T2 H]	3 • Operating CH : CH 8 Frequency : 470.000 MHz [L] 520.000 MHz [H] • Receiving			
	CONVENIENT: The BPF C/L/H can be adjustment automatically. ①-1: Put the cursor on "BPF C/L/H ALL" and then push [ENTER] key. ①-2: The connected PC tunes BPF C/L/H to peak levels. or ②-1: Put the cursor on the one of "BPF C/L/H" as desired. ②-2: Push [ENTER] key to start tuning. ②-3: Repeat ②-1 and ②-2 to perform additional BPF tuning.			
Digital RSSI* [Dig RSSI]	1 • Operating CH. : CH 9 • Connect the SSG to the antenna connector and set as; Frequency : 435.000 MHz [L] 485.000 MHz [H] Level : -20 dB μ [†] (-127 dBm) Modulation : No modulation • Receiving		Put the cursor on "Dig RSSI" and push the [ENTER] key to set the Digital RSSI level.	
S-METER [RSSI]	1 • Operating CH. : CH 4 • Connect the SSG to the antenna connector and set as; Frequency : 435.000 MHz [L] 485.000 MHz [H] Level : +23 dB μ [†] (-84 dBm) Modulation : 1 kHz Deviation : \pm 3.0 kHz • Receiving		Push the [ENTER] key on the connected computer's keyboard to set "S3" level.	
	2 • Set the SSG as; Level : -7dB μ [†] (-114 dBm) • Receiving		Push the [ENTER] key on the connected computer's keyboard to set "S1" level.	
SQUELCH LEVEL [SQL]	1 • Operating CH. : CH 4 • Connect the SSG to the antenna connector and set as; Frequency : 435.000 MHz [L] 485.000 MHz [H] Level : -14dB μ [†] (-121 dBm) Modulation : 1 kHz Deviation : \pm 3.0 kHz • Receiving	Top panel	Connect speaker to the JIG cable.	Set the SQL level to close squelch. Then set SQL level at the point where the audio signals just appears.

[†]: The output level of the standard signal generator (SSG) is indicated as the SSG's open circuit.

*: [IC-F80DT/DS] only

[DSP UNIT] (IC-F80DT/DS only)

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
R64	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	B	5.3/11.6
R65	7030004970	S.RES ERJ2GEJ 470 X (47 Ω)	T	25.7/27.1
R66	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	B	7.3/19.2
R67	7030007290	S.RES ERJ2GEJ 222 X (2.2 kΩ)	T	22/27.3
R68	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	T	20.8/29.1
R70	7030008290	S.RES ERJ2GEJ 183 X (18 kΩ)	T	9.1/10.2
R71	7030005600	S.RES ERJ2GEJ 273 X (27 kΩ)	T	8.2/10.2
R72	7030008290	S.RES ERJ2GEJ 183 X (18 kΩ)	T	7.3/10.2
R73	7030005600	S.RES ERJ2GEJ 273 X (27 kΩ)	T	6.4/9.2
R74	7030005600	S.RES ERJ2GEJ 273 X (27 kΩ)	T	5.5/9.2
R75	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	T	9.3/12.4
R76	7030007340	S.RES ERJ2GEJ 153 X (15 kΩ)	T	8.4/12.4
R77	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	T	7.5/12.9
R78	7030007340	S.RES ERJ2GEJ 153 X (15 kΩ)	T	6.6/12.7
R79	7030007340	S.RES ERJ2GEJ 153 X (15 kΩ)	T	5.7/12
R80	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	B	20.7/35.9
R82	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	3.5/17.2
R83	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	B	2.1/38.6
R85	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	B	4.3/38.8
R86	7030005010	S.RES ERJ2GEJ 681 X (680 Ω)	B	12.1/20.3
R87	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	10.7/18.5
R88	7030004970	S.RES ERJ2GEJ 470 X (47 Ω)	B	9.8/19.8
R89	7030010040	S.RES ERJ2GE-JPW	T	3.3/37.4
R90	7030008370	S.RES ERJ2GEJ 561 X (560 Ω)	T	22/28.9
R91	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	23.4/25.7
R92	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	23.5/24.8
R93	7030010040	S.RES ERJ2GE-JPW	T	22.2/24
R94	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	7.8/19.8
R95	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	17.1/19.6
R96	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	T	1.6/11.8
R97	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	T	1.9/18.6

[DSP UNIT] (IC-F80DT/DS only)

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
C64	4030017460	S.CER ECJ0EB1E102K	T	23/14
C65	4030016930	S.CER ECJ0EB1A104K	T	18.9/17.6
C66	4550007030	S.TAN TEESVP 0J 106M8R		22.4/12.6
C67	4030017490	S.CER C1608 JB 1A 105K-T	T	20/17.2
C68	4030017460	S.CER ECJ0EB1E102K	T	1.2/26.5
C69	4030017460	S.CER ECJ0EB1E102K	T	1.6/38.1
C70	4030017490	S.CER C1608 JB 1A 105K-T	T	20.9/37.9
C71	4030017460	S.CER ECJ0EB1E102K	T	19.2/37.5
C72	4030016930	S.CER ECJ0EB1A104K	B	24.7/19.3
C73	4030016930	S.CER ECJ0EB1A104K	T	25.7/38.9
C74	4030017620	S.CER ECJ0EC1H100C	T	23.3/32.1
C75	4030016930	S.CER ECJ0EB1A104K	T	24.5/32.6
C76	4030017460	S.CER ECJ0EB1E102K	B	4.9/18.8
C77	4030017460	S.CER ECJ0EB1E102K	T	24.8/27.1
C78	4030017460	S.CER ECJ0EB1E102K	B	9.4/21.8
C79	4030017460	S.CER ECJ0EB1E102K	T	18.9/38.7
C80	4030017460	S.CER ECJ0EB1E102K	T	9.3/21.3
C81	4030017460	S.CER ECJ0EB1E102K	T	10.3/13.3
C82	4550007070	S.TAN TEESVP 1A 475M8R	T	2.8/21.9
C83	4030016790	S.CER ECJ0EB1C103K	B	17.4/39.7
C84	4030016930	S.CER ECJ0EB1A104K	T	4.9/21.5
C85	4030016930	S.CER ECJ0EB1A104K	T	2.5/23.3
C86	4030017460	S.CER ECJ0EB1E102K	B	1.2/37.9
C88	4030017730	S.CER ECJ0EB1E471K	B	1.4/23.1
C89	4030017490	S.CER C1608 JB 1A 105K-T	B	2.9/21.9
C90	4030017730	S.CER ECJ0EB1E471K	B	1.5/24.8
C91	4030017730	S.CER ECJ0EB1E471K	B	4.8/4.9
C92	4030016930	S.CER ECJ0EB1A104K	T	21.8/30.5
C93	4030017640	S.CER ECJ0EC1H150J	T	23.3/27.5
C94	4030016930	S.CER ECJ0EB1A104K	T	22.2/25.6
J1	6510018440	S.CNR AXN430C330P	T	13.2/4.3

[FUSE BOARD]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
L1	6200006190	S.COL BLM21PG300SN1D	T	7.5/6.5
C1	4030017460	S.CER ECJ0EB1E102K	T	10.5/2.9
J1	6910016860	CNR IMSA-9230B-1-02H12-PT1		

[VR BOARD]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
R1	7210003200	VAR TP76N937N-16.5F-10KA-2803		
DS1	5040003170	LED UW3804X		
S1	2250000500	ECR TP70TF5164S-20F-2803		

[ANT BOARD]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
L1	6200008330	S.COL 0.45-1.4-4TL 15N	[L]	3.9/10.4
	6200009360	S.COL 0.45-1.4-3TL 11N	[H]	3.9/10.4
C1	4030006980	S.CER C1608 CH 1H 070D-T	[L]	2.6/13
	4030009520	S.CER C1608 CH 1H 020B-T	[H]	2.6/13

[CHASSIS PARTS]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
J1	6910015860	CNR IMSA-6277S-02A-G		
J2	6910016780	CNR ANT CONNECTOR-105		
W1	8900013740	CBL OPC-1429		

[L]=Low band, [H]=High band

M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)
S.=Surface mount

SECTION 7 MECHANICAL PARTS AND DISASSEMBLY

[CHASSIS PARTS]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
J1	6910015860	IMSA-6277S-O2A-G	1
J2	6910016780	ANT connector 105	1
SP1	2510001300	036D0801C	1
W1	8900013740	OPC-1429	1
W2	8900010960	OPC-1129	1
MP1	8210021540	2803 S-front panel	1
	8210021800	2803 T-front panel	1
MP2	8210021490	2803 rear panel	1
MP8	8610012350	Knob N-327	1
MP10	8610012200	Knob N-321 (A)	1
MP17	8010019840	2803 chassis	1
MP20	8930064750	2803 main seal	1
MP22	8930064770	2803 release plate	1
MP25	8930059830	2600 sheet	1
MP26	8930065270	2803 MIC seal	1
MP29	8930059800	2600 pet sheet	1
MP34	8930059360	2600 release button	1
MP35	8930056540	Spring (AH)	2
MP39	8930063690	O-ring (BA)	2
MP41	8930055730	2403 connector seal	1
MP43	8830001470	VR nut (N)	2
MP44	8830002430	2803 ANT nut	1
MP47	8810010480	Screw PH B0 2X6 SUS SSBC	2
MP49	8810010120	Screw PH B0 2X8 SUS ZK	4
MP50	8820001320	2795 screw	2
MP51	8810009510	Screw PH B0 2X4 Ni-Zu (BT)	10
MP52	8810008970	Screw FH B0 2X3.5 Ni-ZU (BT)	2
MP53	8810010430	Screw truss M3X5 SUS SSBC	1
MP55	8930063060	2721 T-rubber	1
MP56	8850002590	2803 ANT washer	1
MP57	8810009180	Screw FH BT B0 2X5 Ni-Zu (BT)	5

[VR BOARD]

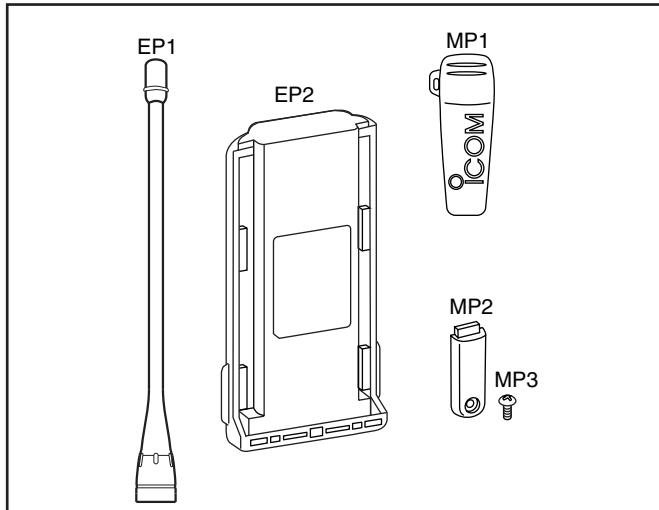
REF NO.	ORDER NO.	DESCRIPTION	QTY.
R1	7210003200	TP76N937N 16.5F A103-2803	1
DS1	5040003170	UW3804X	1
S1	2250000500	TP70TF5164S 20F-2803	1
MP1	8930057690	O ring (AQ)	2

Screw abbreviations

B0, BT: Self-tapping PH: Pan head
NI-ZU: Nickel-Zinc ZK: Black

[ACCESORIES]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
EP1	Optional product	FA-SC57U-1	1
EP2	Optional product	BP-235	1
MP1	Optional product	MB-94	1
MP2	8210021470	2803 side panel	1
MP3	8810010430	Screw truss M3X5 SUS SSBC	1



* Design is depended on versions.

[FRONT UNIT]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
MC201	7700002310	EM-140	1
MP1	8210021460	2803 reflector	1
MP2	8930061120	Shield sponge (AA)	2
MP3	8930062540	Sponge (HO)	2
MP5	8930066040	Sponge (IK)	1
MP6	8930066250	2803 sponge	1
MP7	8930057931	Shield sponge (M)-1	1

[MAIN UNIT]

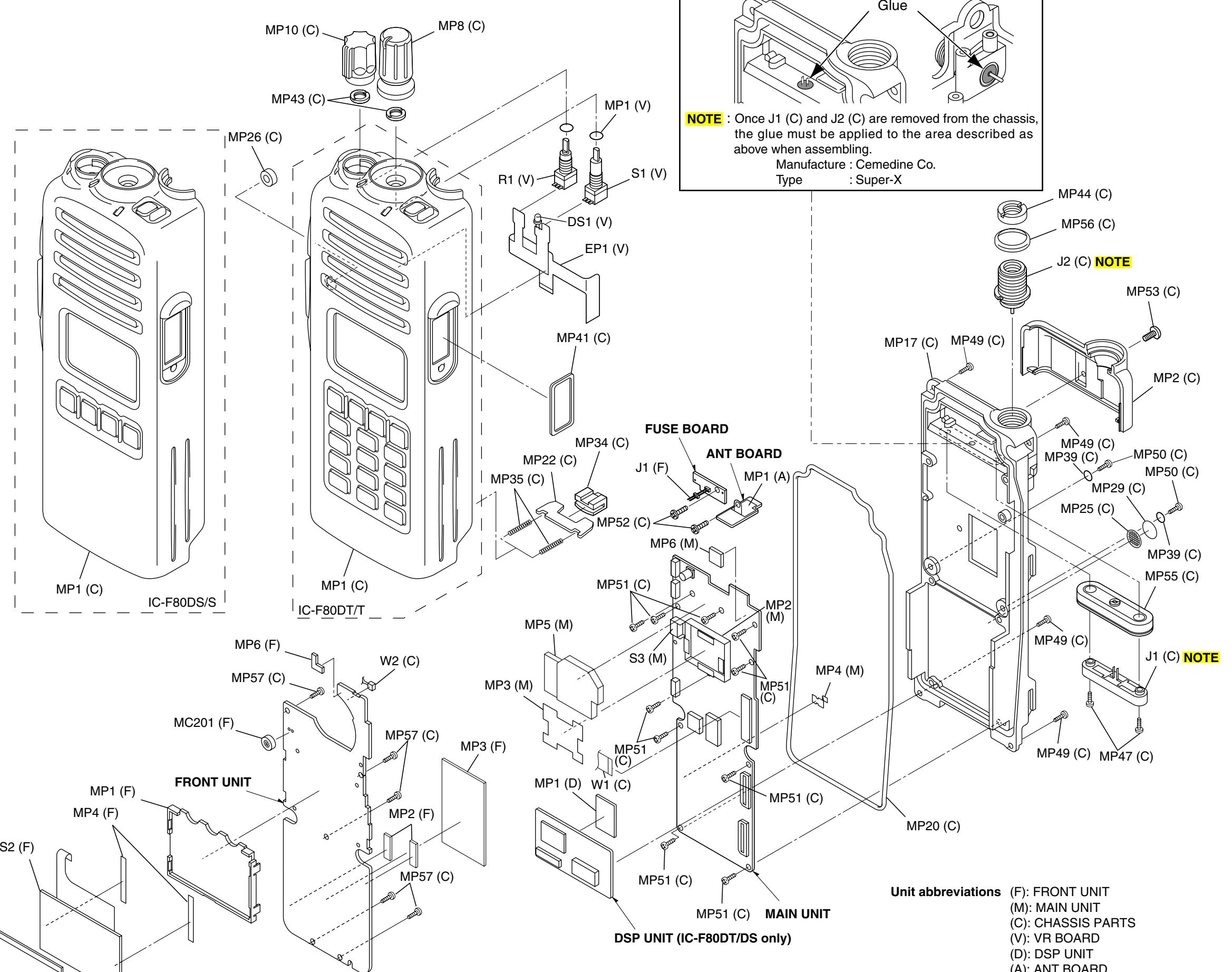
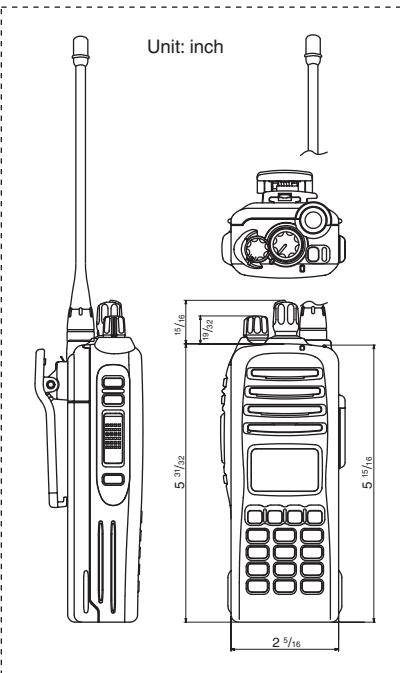
REF NO.	ORDER NO.	DESCRIPTION	QTY.
MP3	8510016870	2803 VCO cover	1
MP5	8510017130	2804 PA shield	1
MP6	8930066240	Sponge (IM)	1

[DSP UNIT] (IC-F80DT/DS only)

REF NO.	ORDER NO.	DESCRIPTION	QTY.
MP1	8930059940	Sponge (HF)	1

[FUSE BOARD]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
J1	6910016860	9230B-1-02H12-Pt1	1



SECTION 8 SEMICONDUCTOR INFORMATION

• TRANSISTORS AND FET'S

2SA1577 T106 Q (Symbol: HQ)	2SB1132 T100 Q (Symbol: BAQ)	2SC3357 T1 RF (Symbol: RF)	2SC4081 T106 R (Symbol: BR)	2SC4116 BL (Symbol: LL)
2SC4116 Y (Symbol: LY)	2SC4215 O (Symbol: QO)	2SC4215 Y (Symbol: QY)	2SC4226 T1 R25 (Symbol: R25)	2SC5006 T1 (Symbol: 24)
2SC5107 O (Symbol: MFO)	2SK1829 (Symbol: K1)	2SK880 Y (Symbol: XY)	3SK293 (Symbol: UF)	DTA114 EE TL (Symbol: 14)
DTA144 EE TL (Symbol: 16)	DTB123 EK T146 (Symbol: F12)	DTC144 EE TL (Symbol: 26)	DTC144EUA T106 (Symbol: 26_)	RD01MUS1 (Symbol: K2)
RD07MVS1 (Symbol: RD07MVS1)	RSR025N03 (Symbol: QY)	TPC6103 (Symbol: S3C)	UMG2N (Symbol: G2)	XP1214 (Symbol: 9H)
XP6501 AB (Symbol: 5N)				

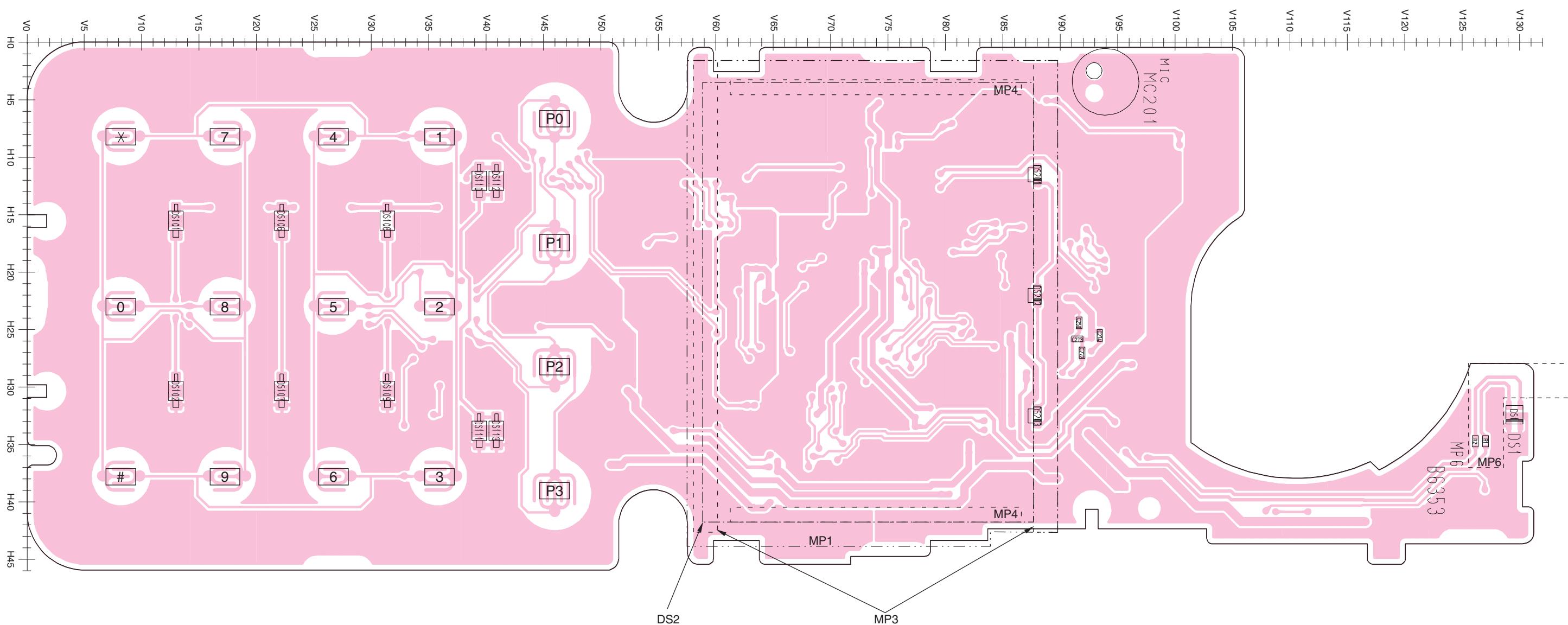
• DIODES

1SS301 (Symbol: B3)	1SV305 (Symbol: TV)	1SV307 (Symbol: TX)	DA221 TL (Symbol: K)	DAN235E TL (Symbol: M)
DAP202 U T106 (Symbol: P)	DAP222 TL (Symbol: P)	HVC350B (Symbol: B0)	MA2S077 (Symbol: S)	MA2S111 (Symbol: A)
MA2S728 (Symbol: B)	MA368 (Symbol: 6L)	MA8051 M (Symbol: 5-1)	NNCD6.2G (Symbol: 62G)	RB706F-40 T106 (Symbol: 3J)

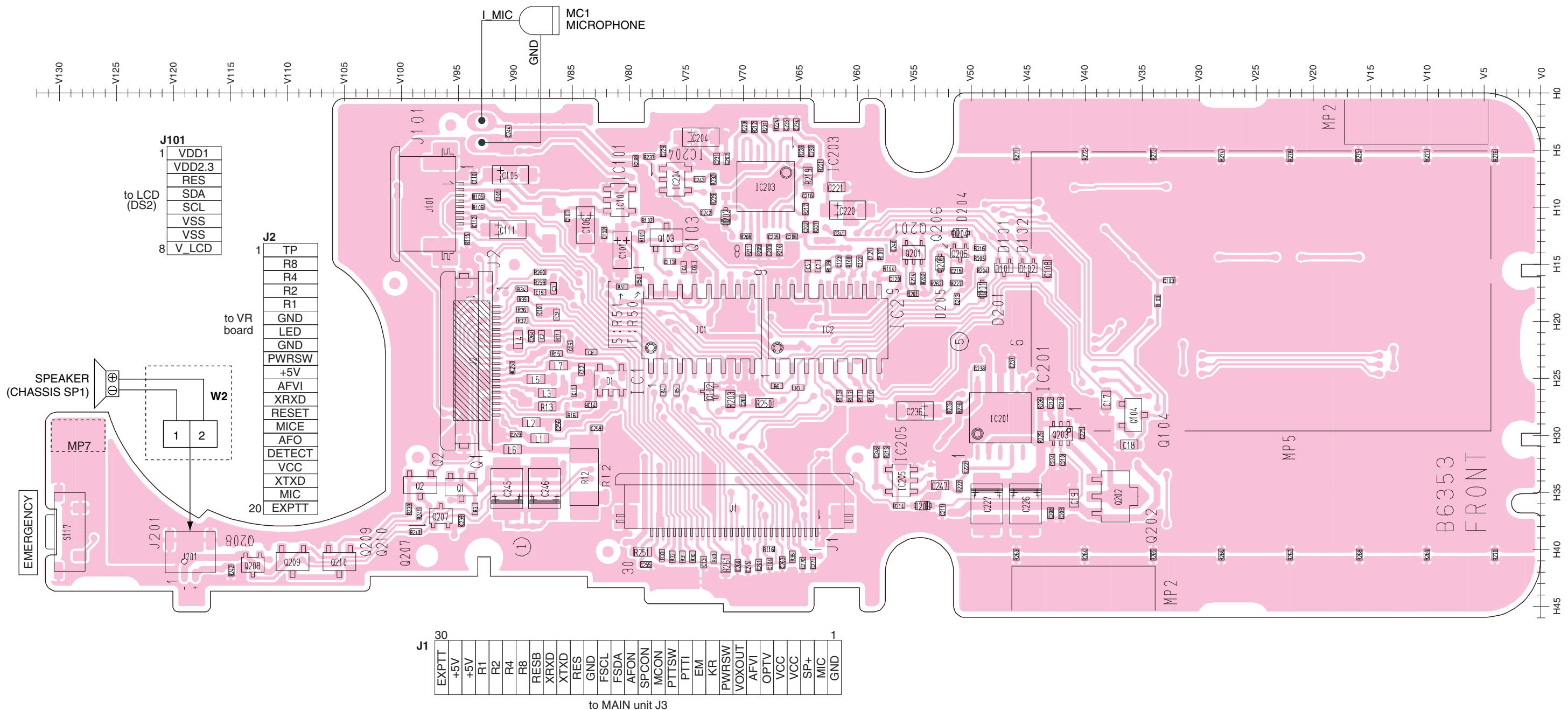
SECTION 9 BOARD LAYOUTS

9-1 FRONT UNIT

• TOP VIEW

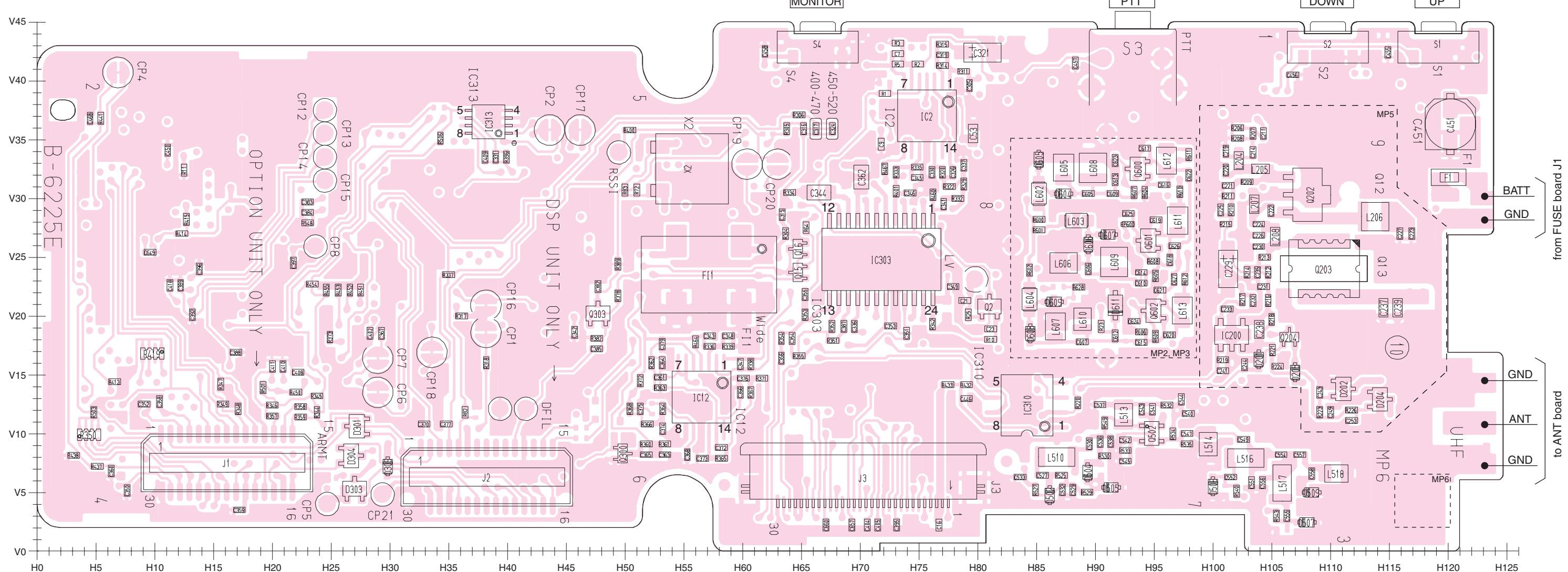


• BOTTOM VIEW (FRONT UNIT)



9-2 MAIN UNIT

• TOP VIEW



1	GND	PTTI
30	CPU5	PTTO
	VCC	MCOT
	AMMT	MCIN
	AFONO	NC
	BEPO	BUSY
	ARMT	NC
	DISC2	SIG
	AFOUT	OPT1
	REM	OPT2
	CCS	OPT3
	IRQA	GND
	CSO	OPV3
	ACSI	OPV2
15	CCK	OPV1
16		

to Optional unit

1	GND	PTTI
30	5V	DPTT
	VCC	DMO
	DIMM	RSSID
	DAFON	DMI
	NC	BUSY
	DRMT	NC
	NC	NC
	DAFO	NC
	NC	NC
	CCS	DFIL
	IRQD	GND
	CSO	DCSI
	CCK	DTXD
15		DRXD
16		

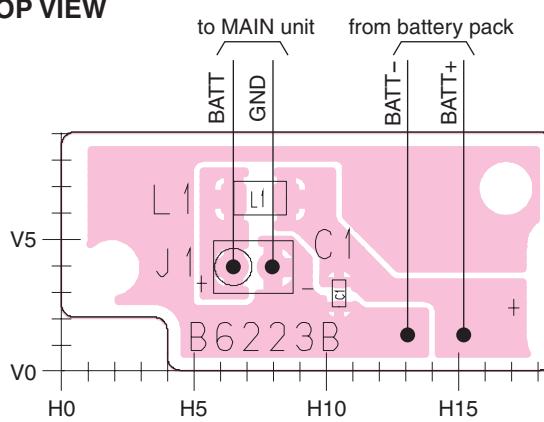
to DSP unit J1

30	GND	MIC
	SP+	VCC
	VCC	VCC
	OPTV	OPTV
	AFVI	VOXOUT
	PTTSW	PWRSW
	MCON	KR
	SPCON	EM
	AFCN	PTTI
	FSDA	MCON
	FSCL	SPCON
	GND	AFCN
	RESET	FSDA
	XTXD	FSCL
	XRXD	GND
	RESB	RESET
	R8	XTXD
	R4	XRXD
	R2	RESB
	R1	R8
	+5V	R4
	+5V	R2
1	EXPTT	R1

to FRONT unit J1

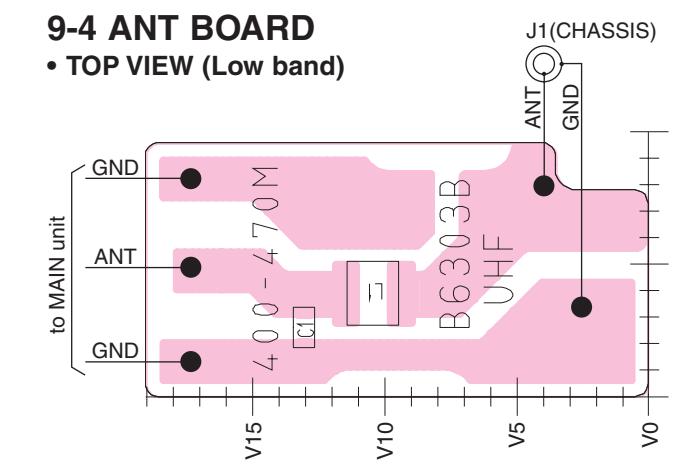
9-3 FUSE BOARD

• TOP VIEW

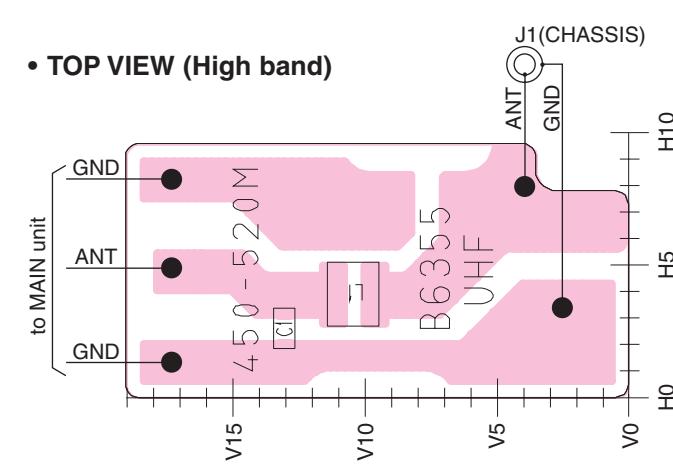


9-4 ANT BOARD

• TOP VIEW (Low band)



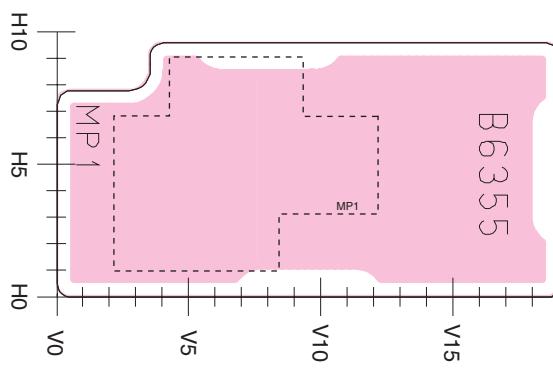
• TOP VIEW (High band)



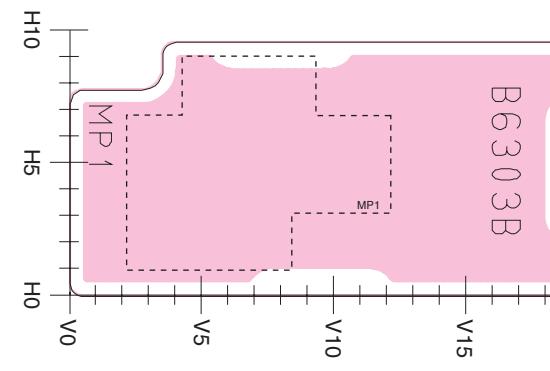
• BOTTOM VIEW (MAIN UNIT)



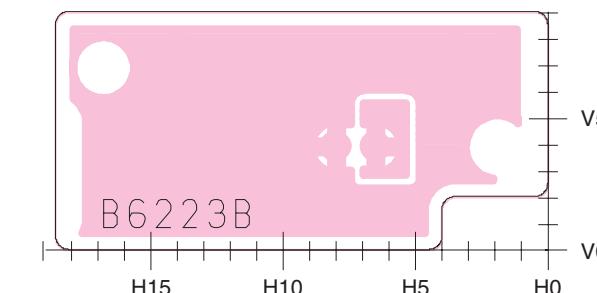
• TOP VIEW (ANT BOARD)
(High band)



• TOP VIEW (ANT BOARD)
(Low band)

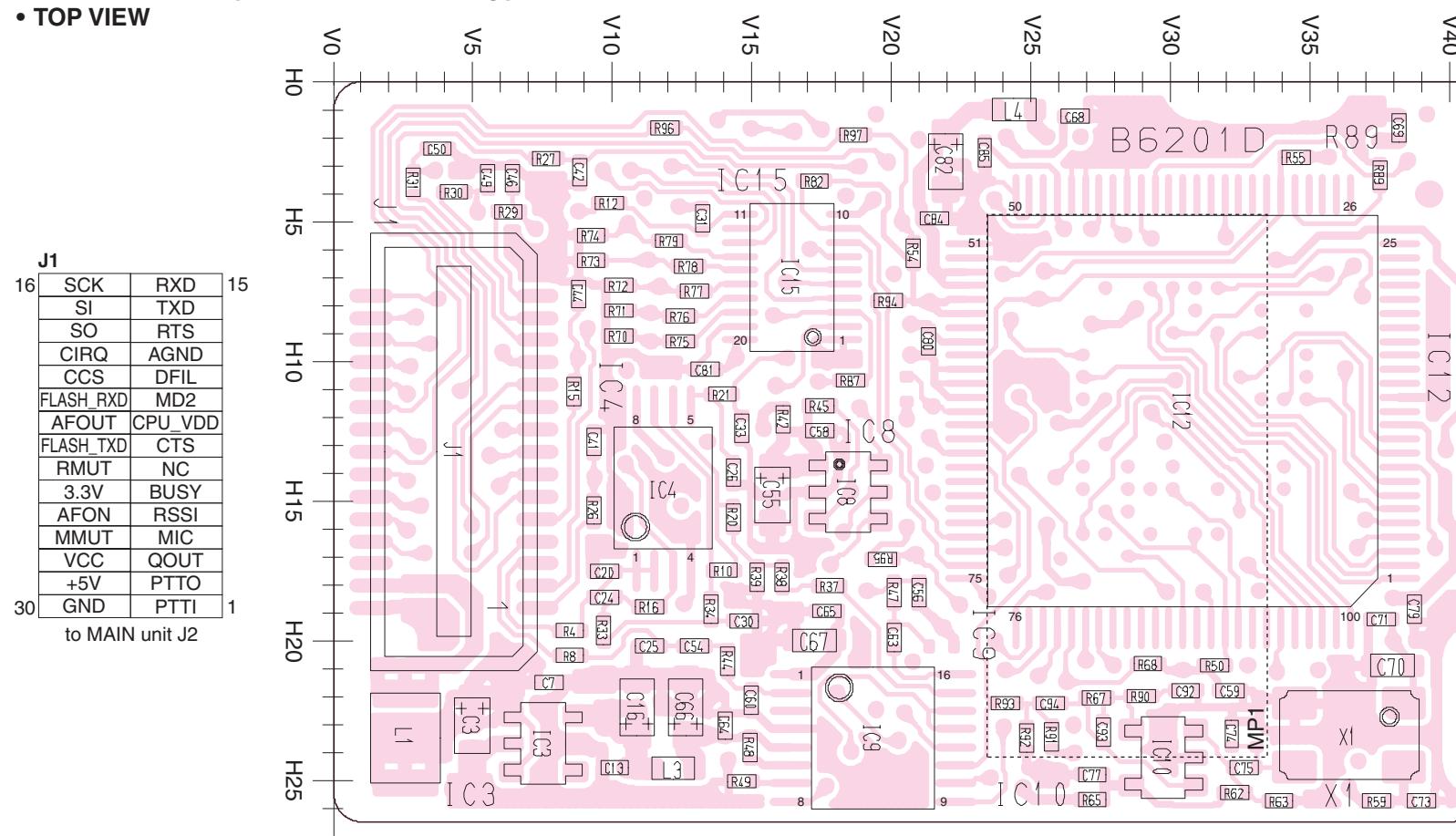


• BOTTOM VIEW (FUSE BOARD)

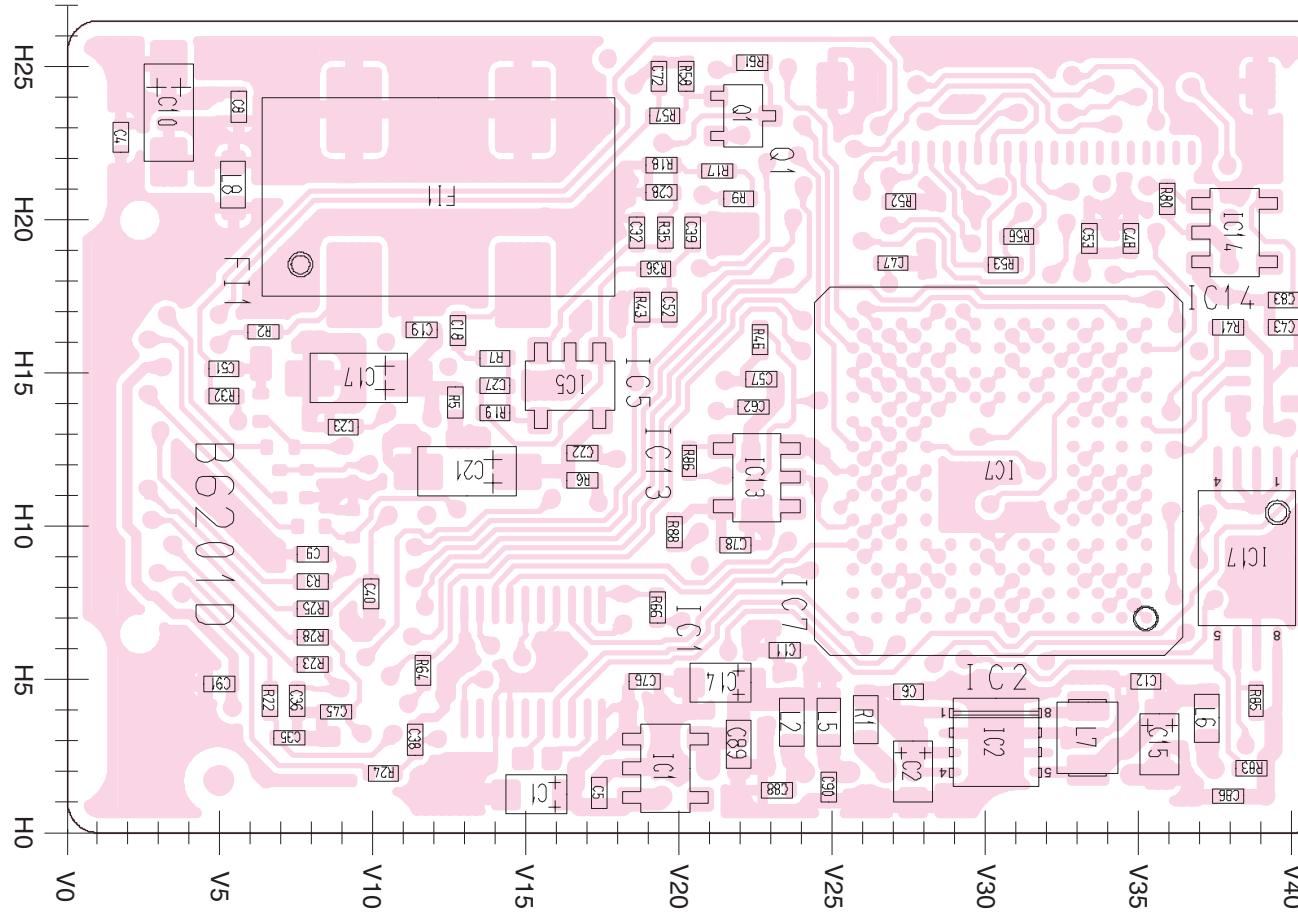


9-5 DSP UNIT (IC-F80DT/DS only)

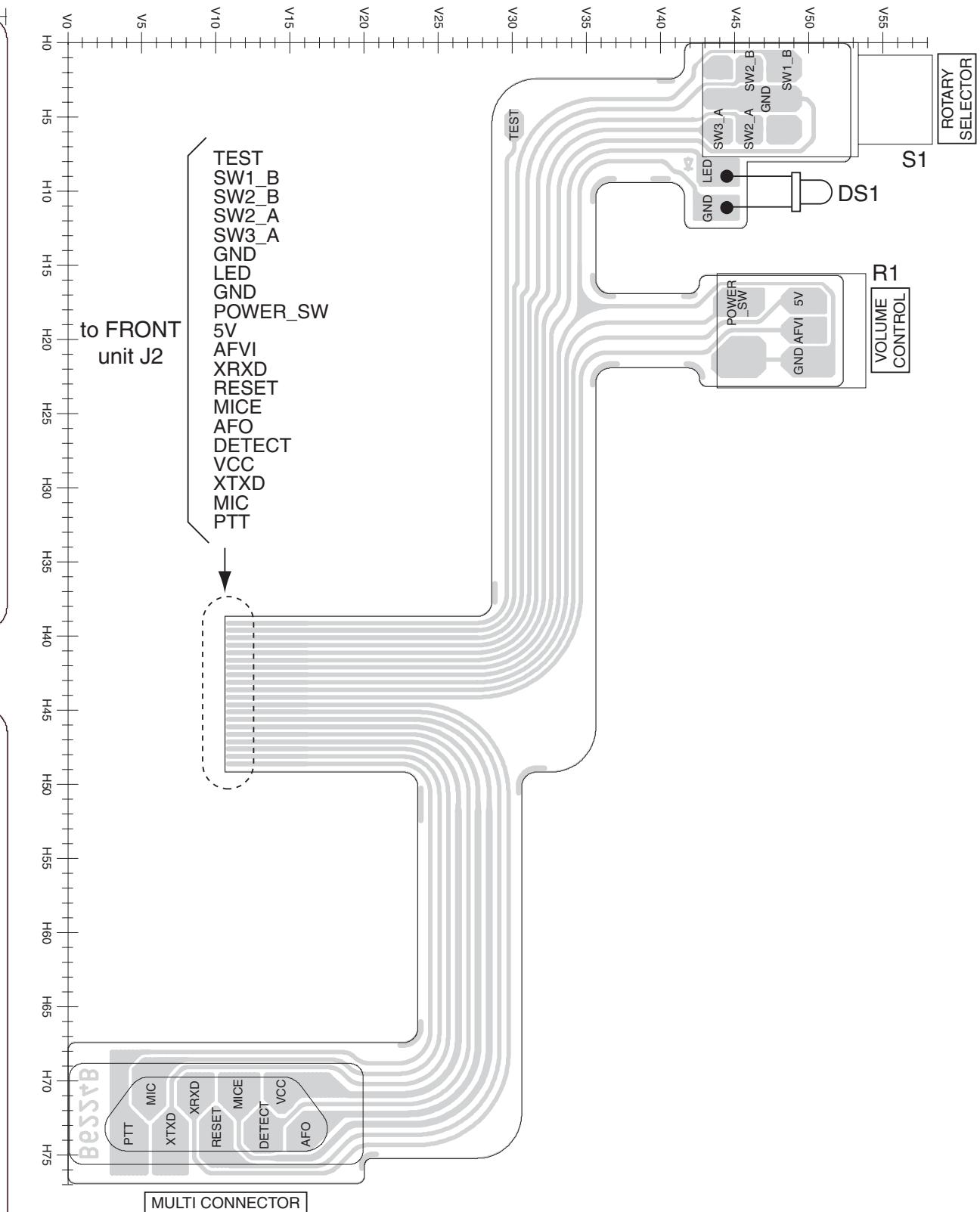
• TOP VIEW



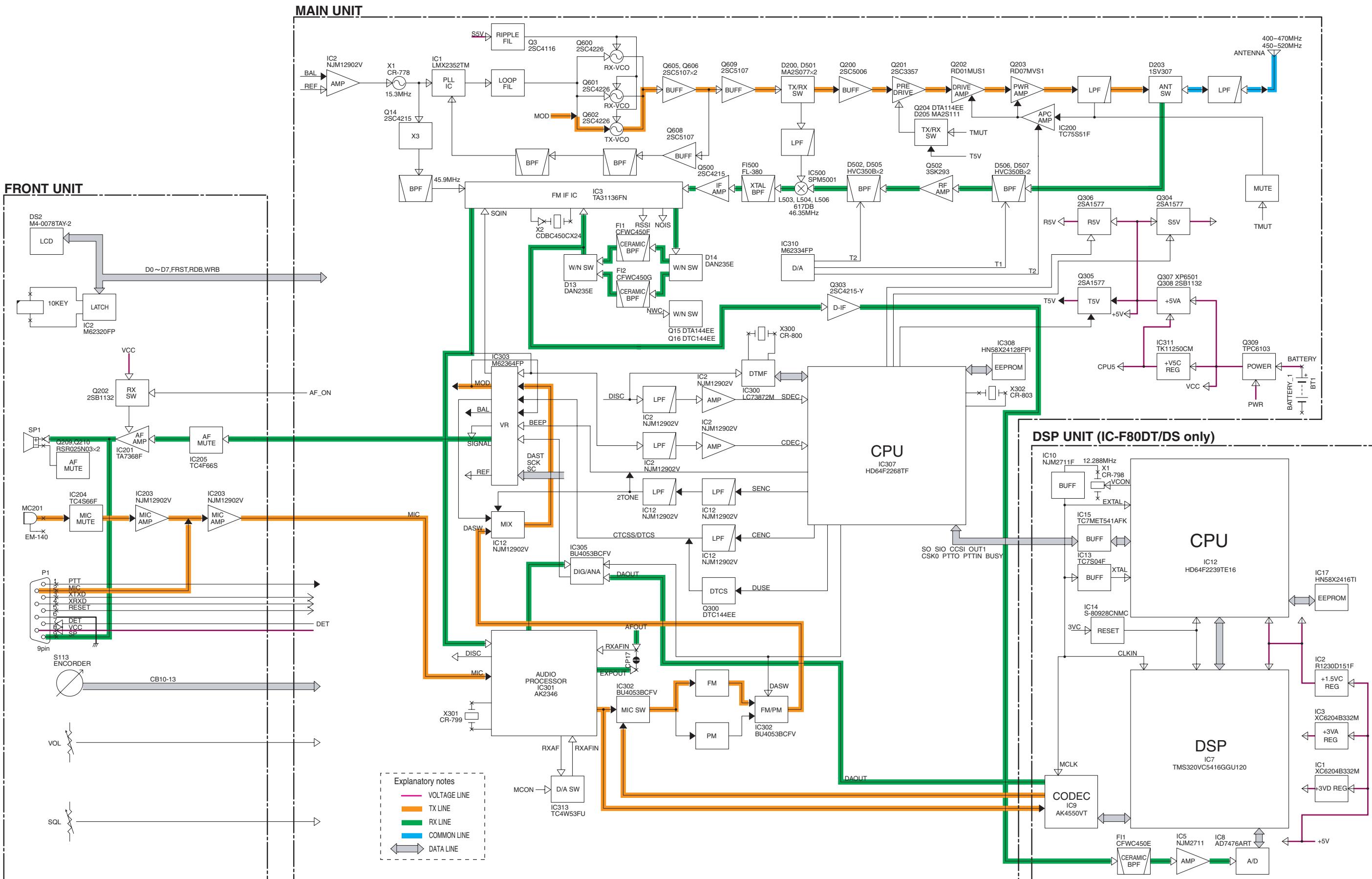
• BOTTOM VIEW (DSP UNIT)



9-6 VR BOARD

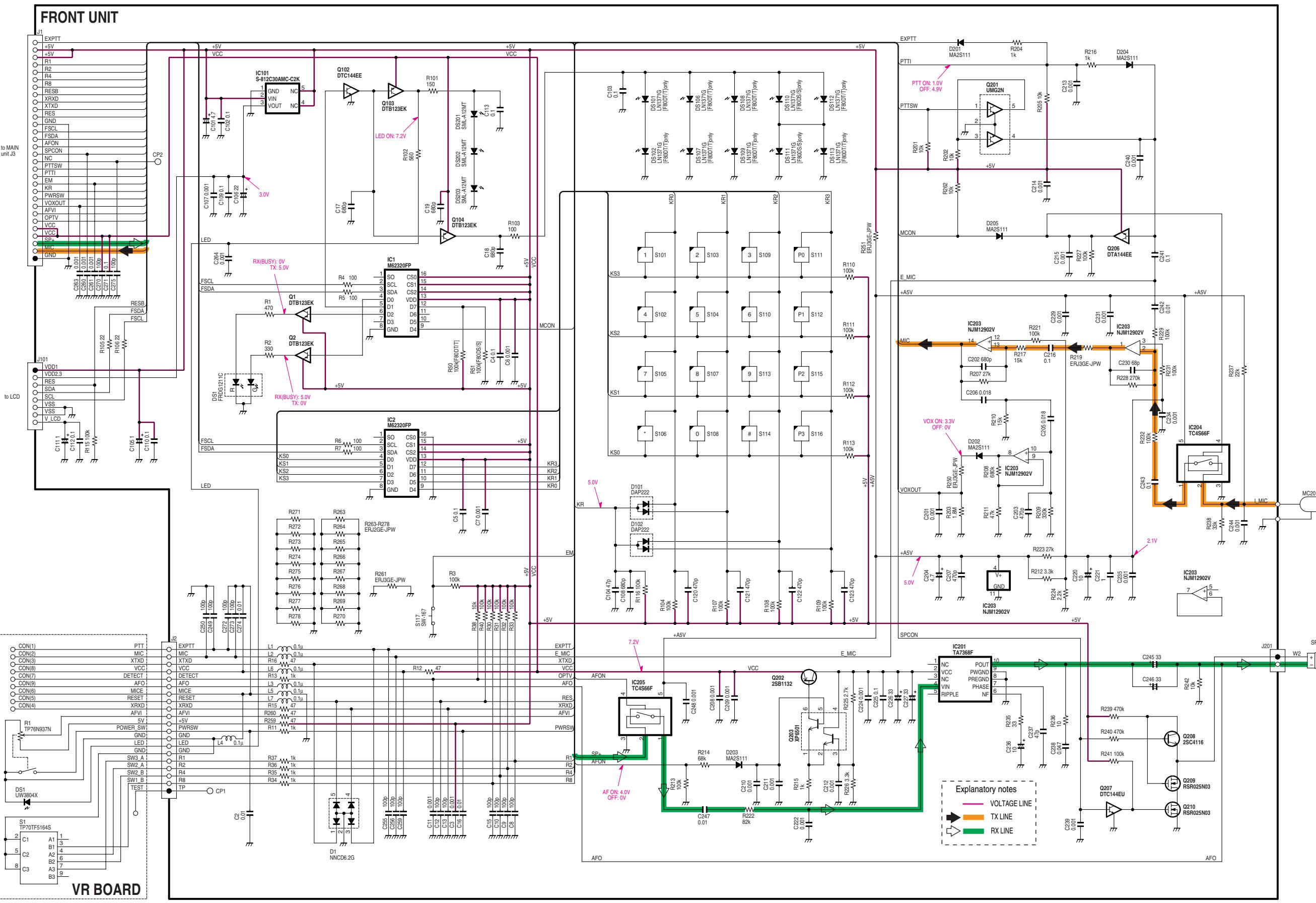


SECTION 10 BLOCK DIAGRAM

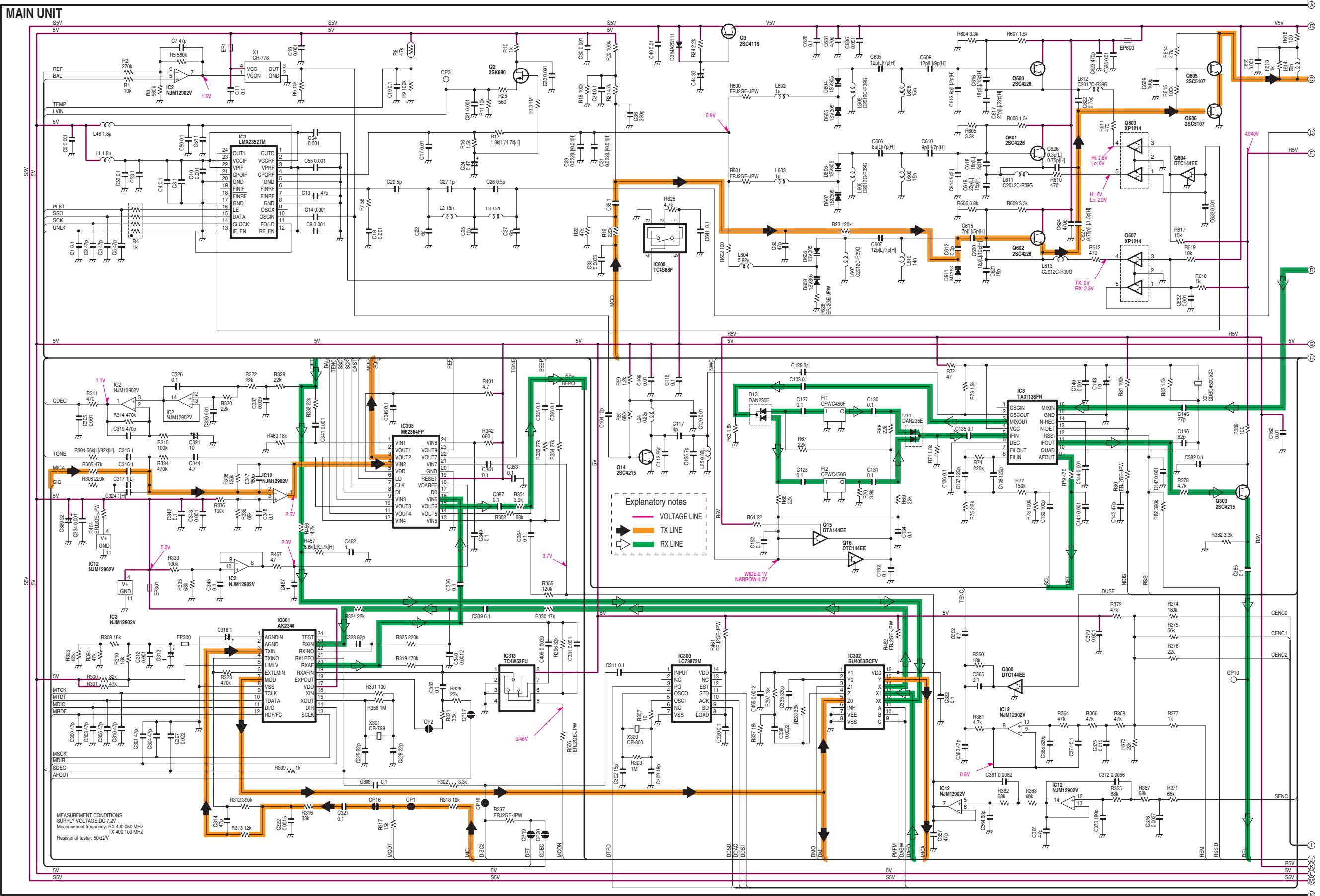


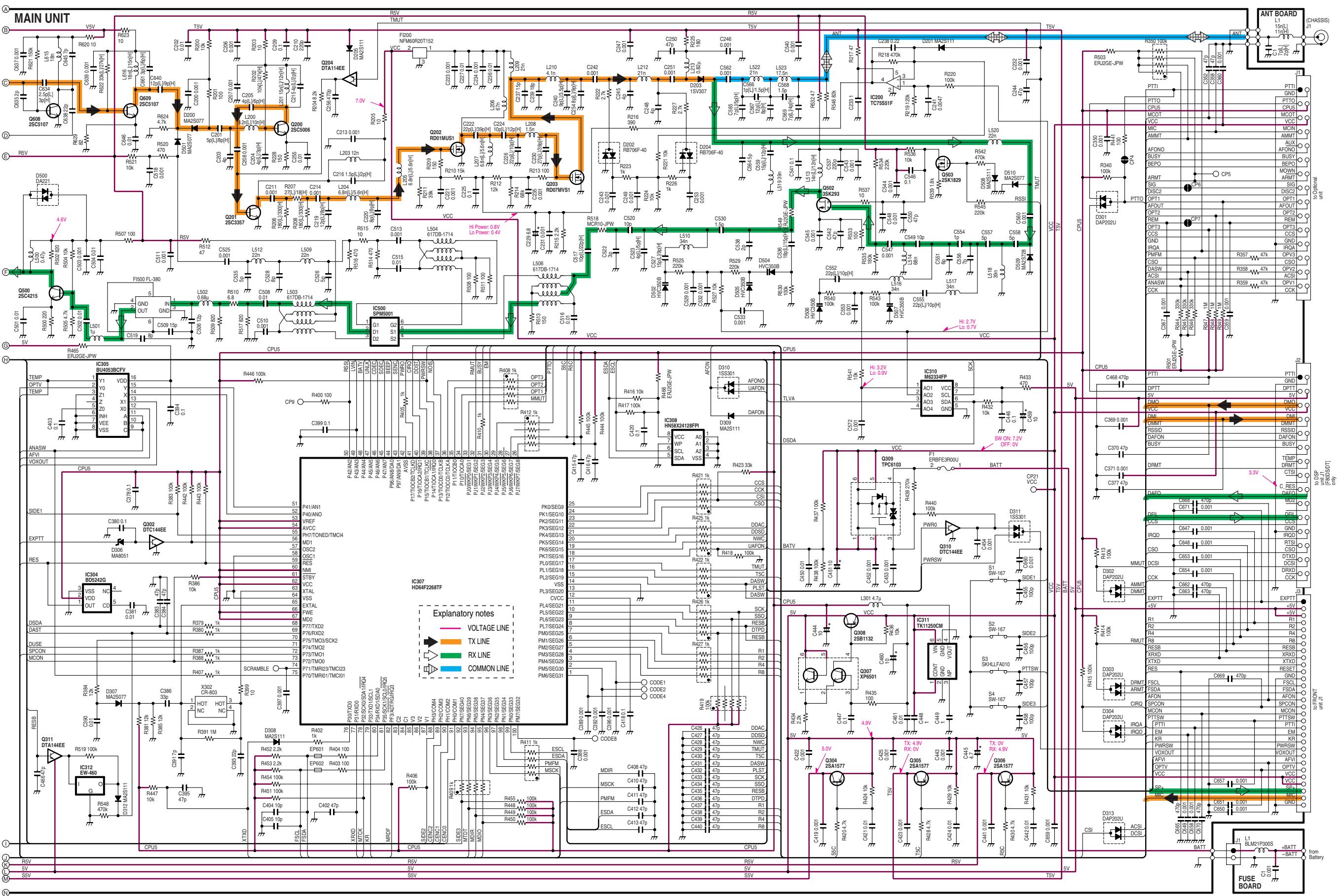
SECTION 11 VOLTAGE DIAGRAMS

11-1 FRONT UNIT

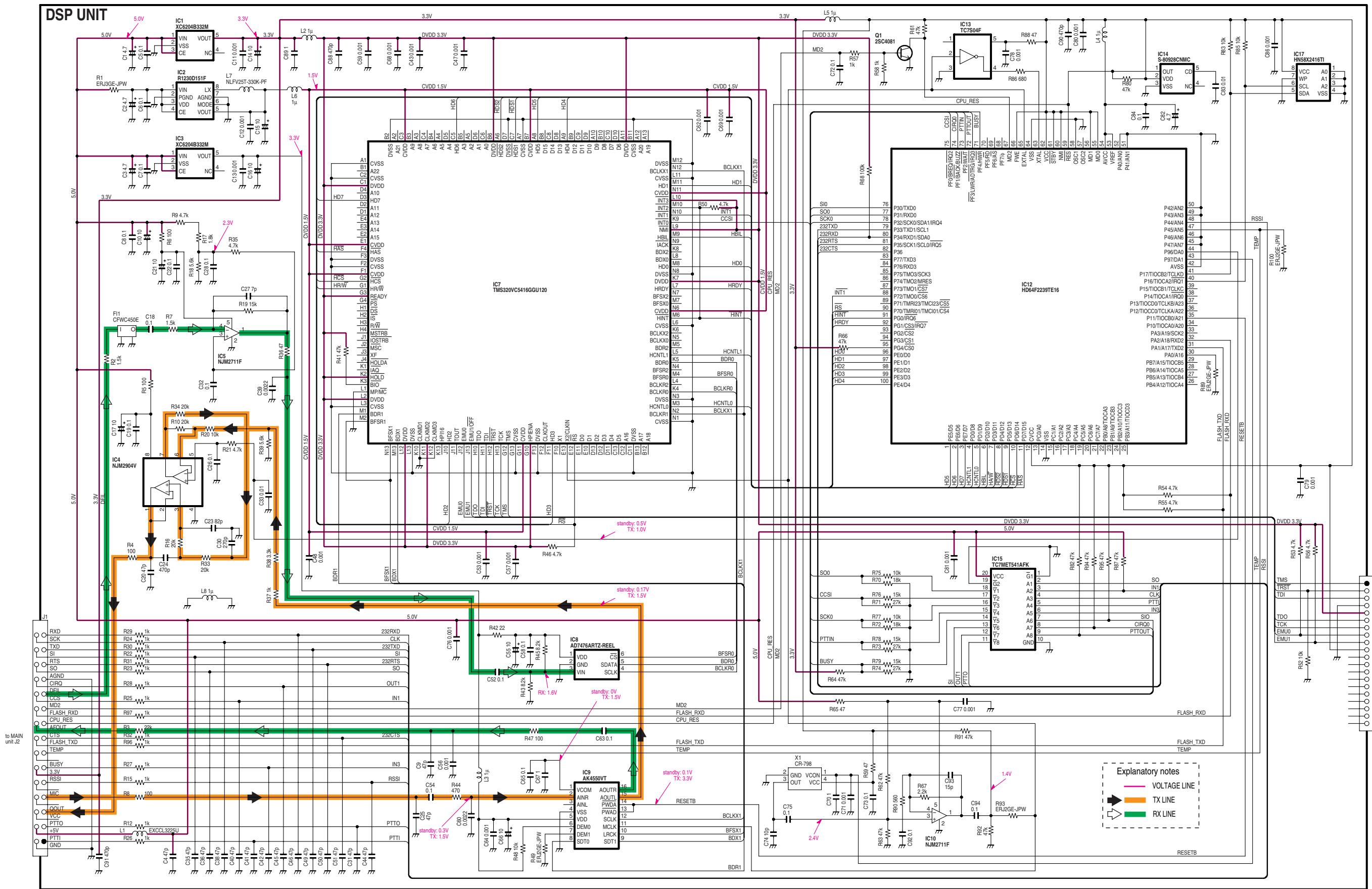


11-2 MAIN UNIT





11-3 DSP UNIT (IC-F80DT/DS only)



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