CIRCUIT DESCRIPTION

Frequency configuration

The receiver utilizes double conversion. The first IF is 38.850 MHz and the second IF is 450kHz. The first local oscillator signal is supplied from the PLL circuit.

The PLL circuit in the transmitter generates the necessary frequencies. Fig. 1 shows the frequencies.

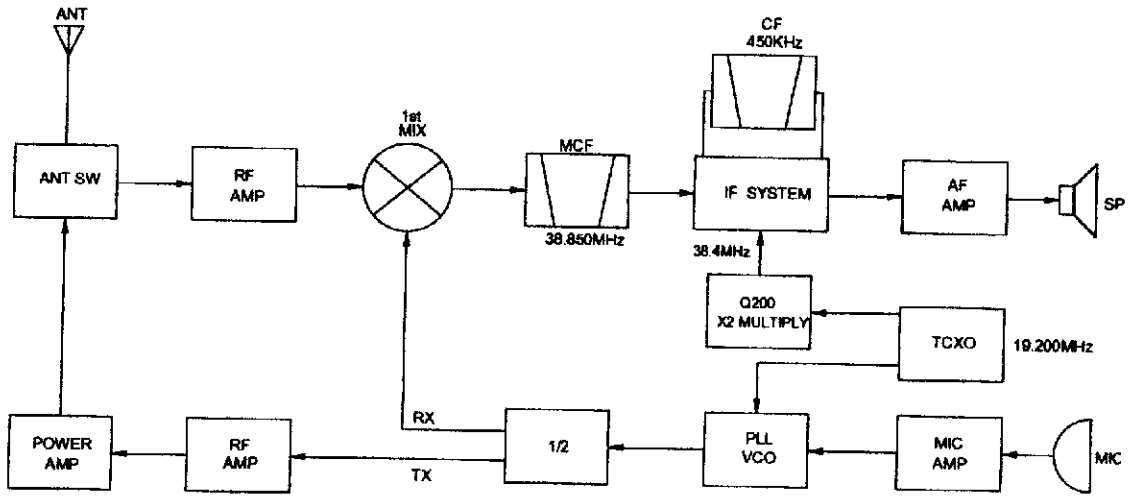


Fig. 1 Frequency configuration

Receiver

The receiver is double conversion super heterodyne, designed to operate in the frequency range of 400 to 490MHz.

The frequency configuration is shown in Fig. 1.

■ Front - end RF amplifier

An incoming signal from the antenna is applied to an RF amplifier (Q206) after passing through a transmit/receive switch circuit (D213 are off) and a band pass filter (L207, L208, L211 and varactor diodes : D207, D208, D209). After the signal is amplified (Q206), the signal is filtered through a band pass filter (L205, L206 and varactor diodes: D205, D206) to eliminate unwanted signals before it is passed to the first mixer.

The voltage of these diodes are controlled by tracking the CPU (U2) center frequency of the band pass filter. (See Fig. 2.)

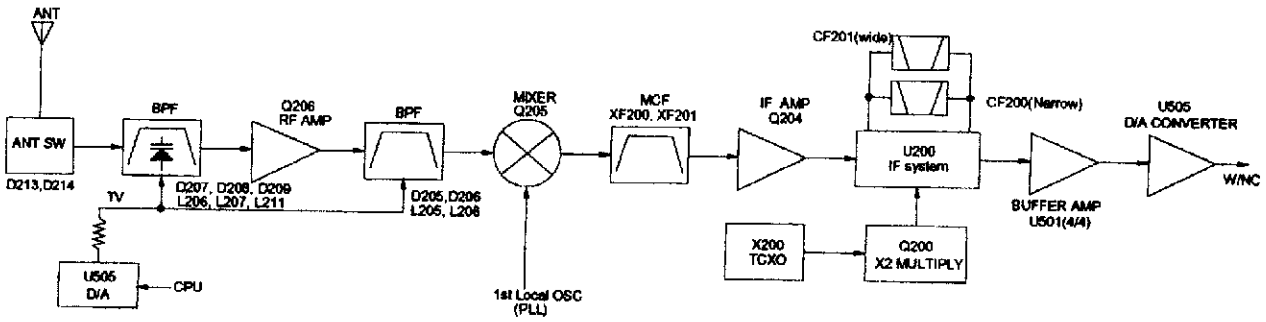


Fig. 2 Receiver section configuration

CIRCUIT DESCRIPTION

■ First Mixer

The signal from the RF amplifier is heterodyned with the first local oscillator signal from the PLL frequency synthesizer circuit at the first mixer (Q205) to create a 38.850MHz first intermediate frequency (1st IF) signal. The first IF signal is then fed through one pair of monolithic crystal filter (MCF : XF200 and XF201) to further remove spurious signals.

■ IF amplifier

The first IF signal is amplified by Q204, and then goes to U200 (FM processing IC). The signal is heterodyned again with a second local oscillator signal within U200 to create a 450kHz second IF signal. The second IF signal is then fed through a 450kHz ceramic filter (Wide : CF201, Narrow : CF200) to further eliminate unwanted signals before it is amplified and FM detected in U200.

■ Wide/Narrow Switching Circuit

The Wide port and Narrow port (pin 35) of the CPU is used to switch between ceramic filters. When the Wide port is high, the ceramic filter SW diodes (D200, D201) cause CF201 to turn on to receive a Wide signal.

When the Narrow port is low, the ceramic filter SW diodes (D200, D201) cause CF200 to turn on to receive a Narrow signal. (See Fig. 3.)

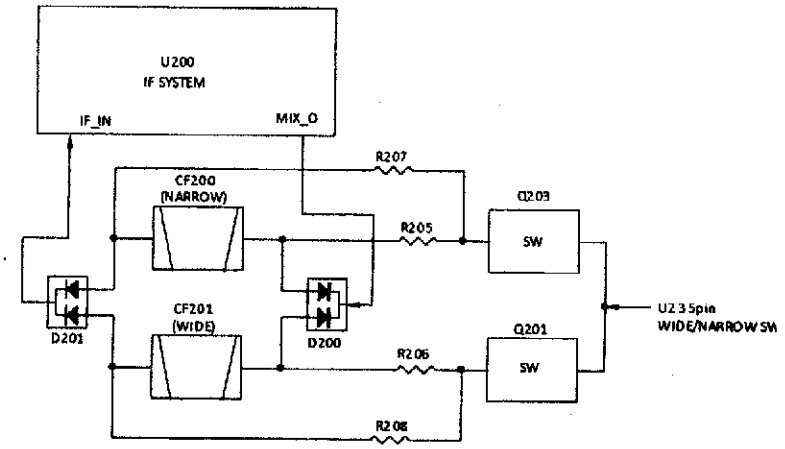


Fig. 3 Wide/Narrow Switching Circuit

■ AF Signal System

The detection signal from IF IC (U200) goes to D/A converter (U505) for adjusting the gain and is output to AF filter (U502) for characterizing the signal. It is also amplified by entering compander amplifier (U500). The AF signal output from U500 and the TONE signal are summed up and the resulting signal goes to the D/A converter (U505). The AFO output level is adjusted by the D/A converter. The signal output from the D/A converter is input to the audio power amplifier (U506). The AF signal from U505 was inputted into (U506).The AF signal from (U506) switches between the internal speaker and speaker jack (J502) output. (See Fig. 4.)

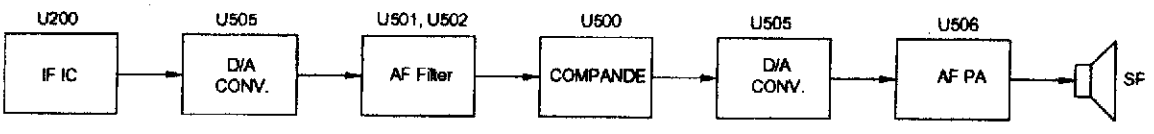


Fig. 4 AF signal system

CIRCUIT DESCRIPTION

■ Squelch Circuit

The detection output from the FM IF IC (U200) passes through a noise amplifier (U201 2/2) to detect noise. A voltage is applied to the CPU (U2). The CPU controls squelch according to the voltage (SQIN) level. The signal from the RSSI pin of U200 is used for S-meter. The electric field strength of the receive signal can be known before the SQIN voltage is input to the CPU, and the scan stop speed is improved.

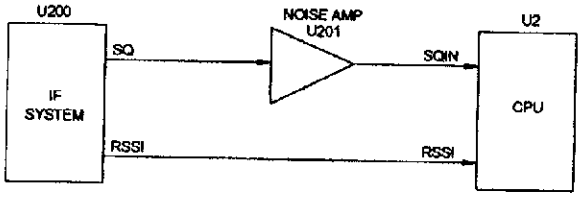


Fig. 5 Squelch Circuit

PLL frequency synthesizer

The PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission.

■ PLL

The frequency step of the PLL circuit is 5 or 6.25kHz. A 19.200MHz reference oscillator signal is divided at U205 by a fixed counter to produce the 5 or 6.25kHz reference frequency. The voltage controlled oscillator (VCO) output signal is buffer amplified by Q210, then divided in U205 by a dualmodule programmable counter. The divided signal is compared in phase with the 5 or 6.25kHz reference signal in the phase comparator in U205. The output signal from the phase comparator is filtered through a low-pass filter and passed to the VCO to control the oscillator frequency. (See Fig. 6.)

■ VCO

The operating frequency is generated by Q217 in transmit mode and Q216 in receive mode. The oscillator frequency is controlled by applying the VCO control voltage, obtained from the phase comparator, to the varactor diodes (D219 and D221 in transmit mode and D218 and D220 in receive mode). The TX/RX pin is set high in receive mode causing Q202 and Q218 to turn Q217 off, and turn Q216 on. The TX/RX pin is set low in transmit mode. The outputs from Q216 and Q217 are amplified by Q210 and sent to the RF amplifiers. (See Fig. 6.)

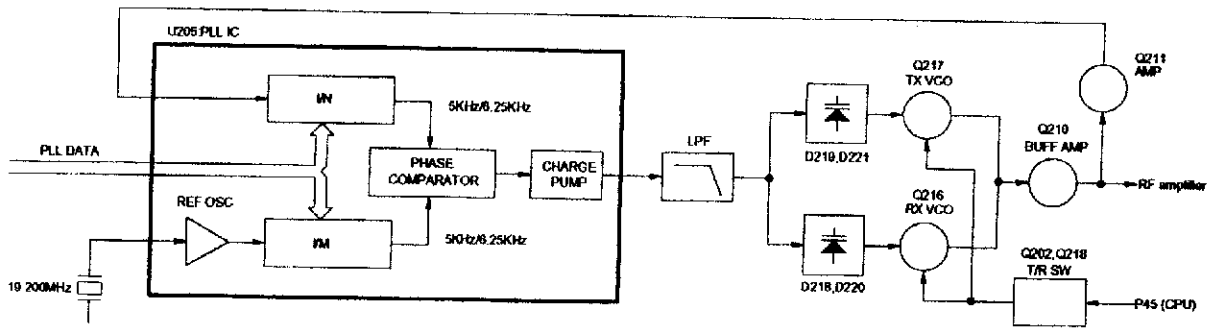


Fig. 6 PLL circuit

■ UNLOCK Circuit

During reception, the RXC signal goes high, the TXC signal goes low, and Q108 turns on. Q101 turns on and a voltage is applied to (8R). During transmission, the RXC signal goes low, the TXC signal goes

CIRCUIT DESCRIPTION

high and Q104 turns on. Q102 turns on and a voltage is applied to (8T).

The CPU in the control unit monitors the PLL (U205) LD signal directly. When the PLL is unlocked during transmission, the PLL LD signal goes low. The CPU detects this signal and makes the TXC signal low. When the TXC signal goes low, no voltage is applied to 8T, and no signal is transmitted. (See Fig. 7.)

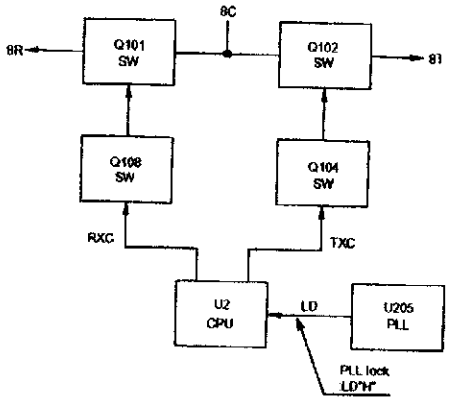


Fig. 7 Unlock circuit

Transmitter

■ Outline

The transmitter circuit produces and amplifies the desired frequency directly. It FM-modulates the carrier signal by means of a varicap diode.

■ Power Amplifier Circuit

The transmit output signal from the VCO passes through the transmission/reception selection diode (D202) and amplified by Q208, Q219, Q212 and Q214. The amplified signal goes to the final amplifier (Q215) through a low-pass filter. The low-pass filter removes unwanted high-frequency harmonic components, and the resulting signal is transmitted through the antenna terminal. (See Fig. 8.)

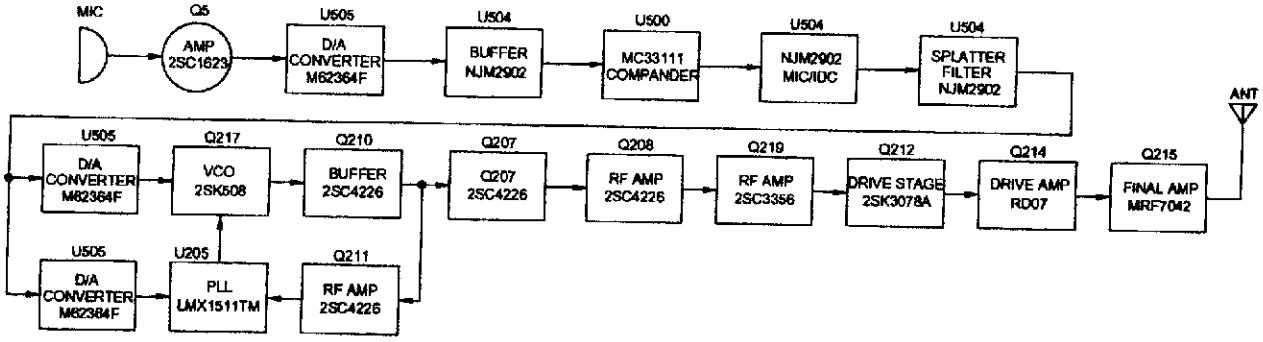


Fig. 8 Transmitter system

■ APC Circuit

The automatic transmission power control (APC) circuit detects part of a final amplifier output with a diode (D228, D229) and applies a voltage to U202. U202 compares the APC control voltage (PC) generated by the D/A converter (U505) with the detection output voltage. U202 generates the voltage to control Q214 and Q215 and stabilizes transmission output.

The APC circuit is configured to protect over current of Q214 and Q215 due to fluctuations of the load

CIRCUIT DESCRIPTION

at the antenna end and to stabilize transmission output at voltage and temperature variations. (See Fig. 9.)

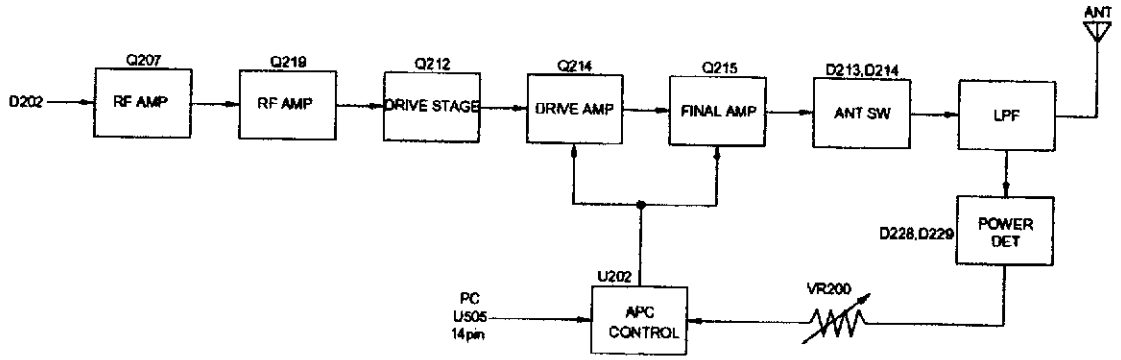


Fig. 9 APC Circuit

Control Circuit

The CPU carries out the following tasks (See Fig. 10.):

1) Controls the WIDE, NARROW, TX/RX outputs.
2) Controls the display unit.
3) Controls the PLL (U205).
4) Controls the D/A converter (U505) and adjusts the volume, modulation and transmission power.

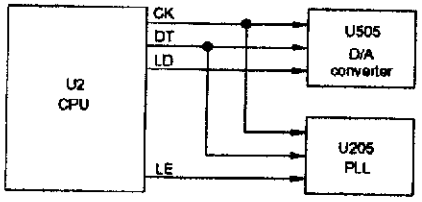


Fig. 10 Control circuit

■ Memory Circuit

The transceiver has an 64k-bit EEPROM (U6). The EEPROM contains adjustment data. The CPU (U2) controls the EEPROM through two serial data lines. (See Fig. 11.)

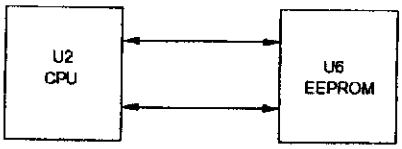


Fig. 11 APC Circuit

■ Display Circuit

The CPU (U2) controls the display LCD and LEDs. When power is on, the CPU will use the P07 line to control the LCD illumination backlight LEDs.

The brightness function is controlled by the switch Q6 and Q7.

The LCD driver (U3) and CPU (U2) communicate through the P85, P86 lines. (See Fig. 12.)

CIRCUIT DESCRIPTION

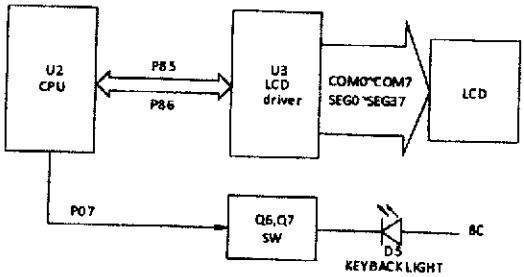


Fig. 12 Display circuit

■ Encode

CTCSS, DCS data of the P31 Line is output from pin 42 of the CPU. The signal passes through a low-pass CR filter and goes to the D/A converter (U505).

High-speed data (2T/5T/DTMF) is output from pin 58 of the CPU. The signal passes through a low-pass CR filter, providing TX and SP output audio frequency, and has processed IDC after amplified by a U504(B/4). The signal then passes through a low-pass filter (separation filter) U504 (C/4 and D/4), and filter the parts which are higher than 3kHz frequency, and the signal attained goes into the D/A converter (U505).

The D/A converter (U505) adjusts the balance between the MOD and CTCSS/DCS levels. Signal of CTCSS/DCS port is summed with MOD and the resulting signal goes to the VCO. This signal is applied to a varicap diode in the VCO for direct FM modulation. (See Fig. 13.)

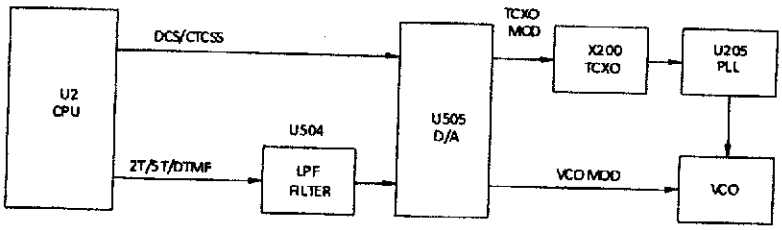


Fig. 13 Encode circuit

■ Decode

DCS/CTCSS/DTMF/2T/5T

The signal from (AFWN) entering into AF signal and higher audio frequencies output by pin 1 of U501: A are cut by low-pass filter U503 and amplified. then led to pin 51 of CPU. The input signal is compared with the programmed tone frequency code in the CPU. The squelch will open when they match.

The signal (DTMF-DET) goes to P02 (pin 52) of CPU (U2). The DTMF/2T/5T input signal from the DTMF-DET goes to compared U2008. The compared signal goes to the CPU for processing and be decoded within the CPU (U2). (See Fig. 14.)

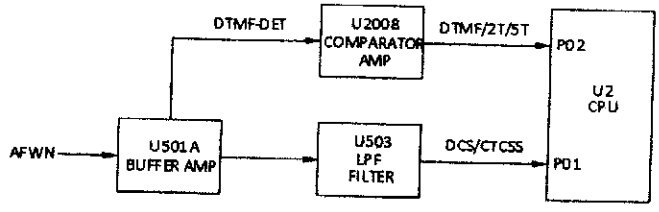


Fig. 14 Decode circuit

CIRCUIT DESCRIPTION

■ D/A Converter

The D/A converter (U505) is used to adjust MO modulation, AF volume, TV voltage, FC reference voltage, and PC POWER CONTROL voltage level.
Adjustment values are sent from the CPU as serial data. The D/A converter has a resolution of 256 and the following relationship is valid.

Power Supply Circuit

When the POWER switch on the display unit is pressed, the power port on the display unit which is connected to CPU port 45 (POWER), goes low, then CPU port 23 (P20) goes high, Q103 turns on, SBE SW (Q100) turns on and power (SBE) is supplied to the radio.

During receiving, the CPU port 19 (P24) output "H" level. Q101 and Q108 turn on. and reception circuit is supplied by 8V power supply (8R).

When the receiving is at FM, the CUP port 16 (P27) output "L" level. Q106 turns on and supplies 8V power supply to FM reception circuit (VFM).

During transmitting, CPU port 18 (P25) output "H" level. Q102 and Q104 turn on. Transmitting circuit output 8V power supply (8T). (See Fig. 15.)

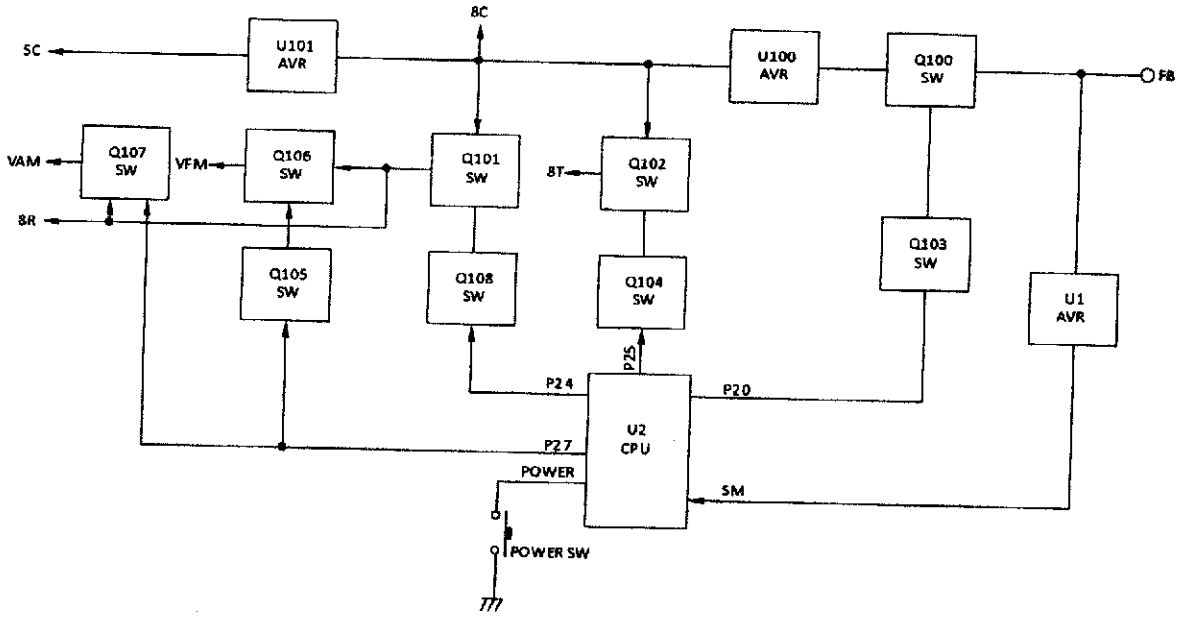
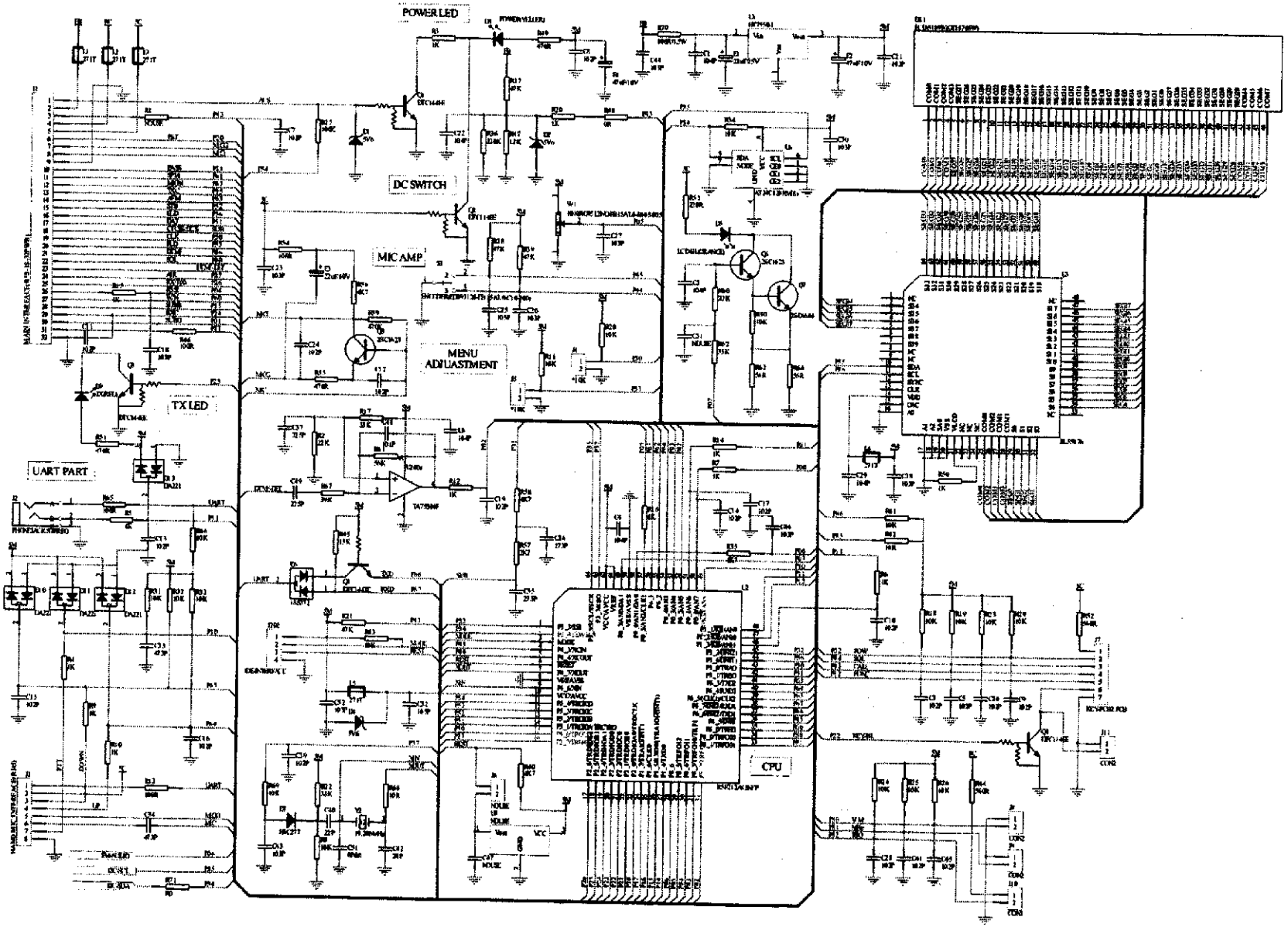


Fig. 15 Power supply circuit

SCHEMATIC DIAGRAM



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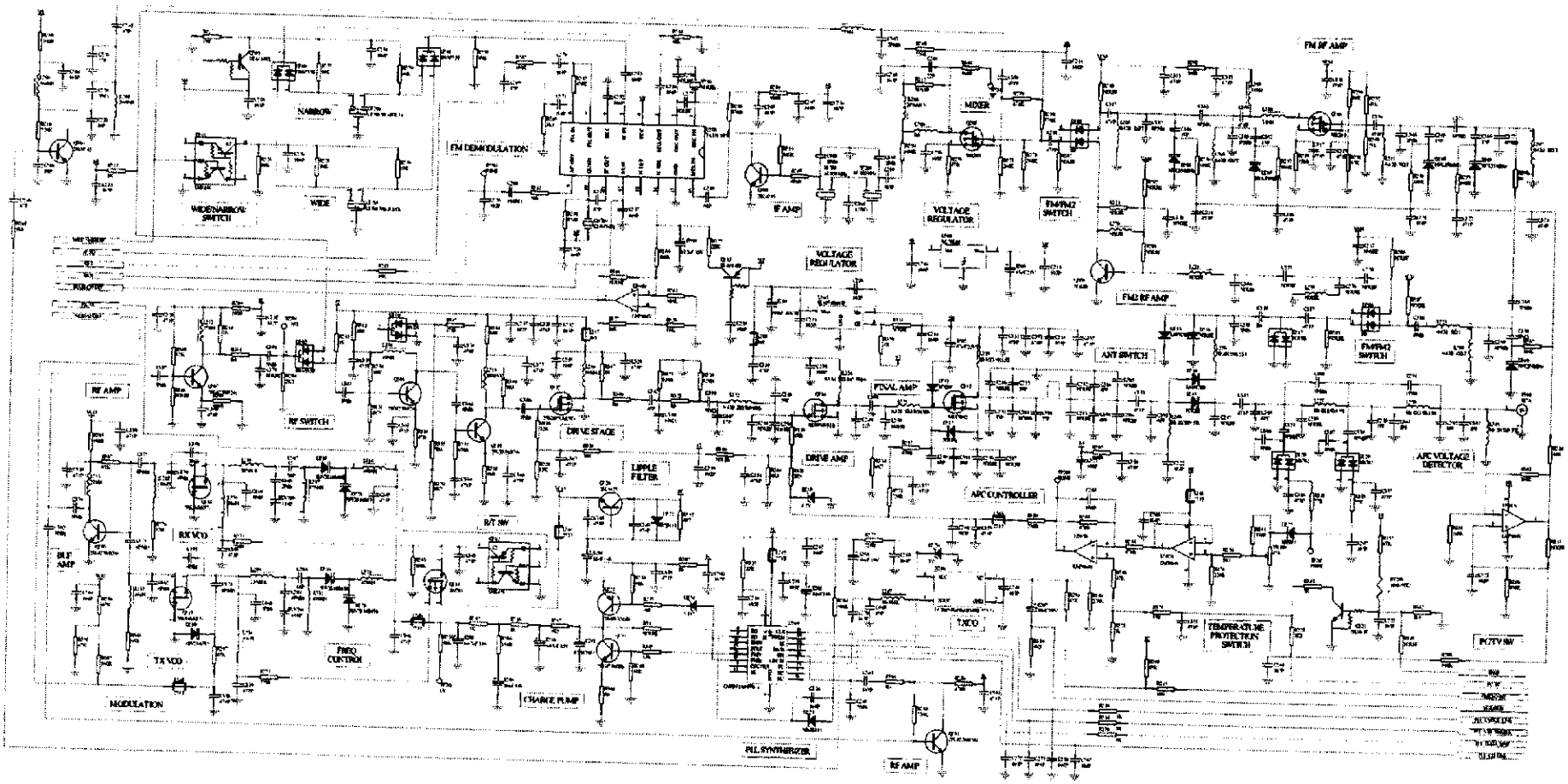

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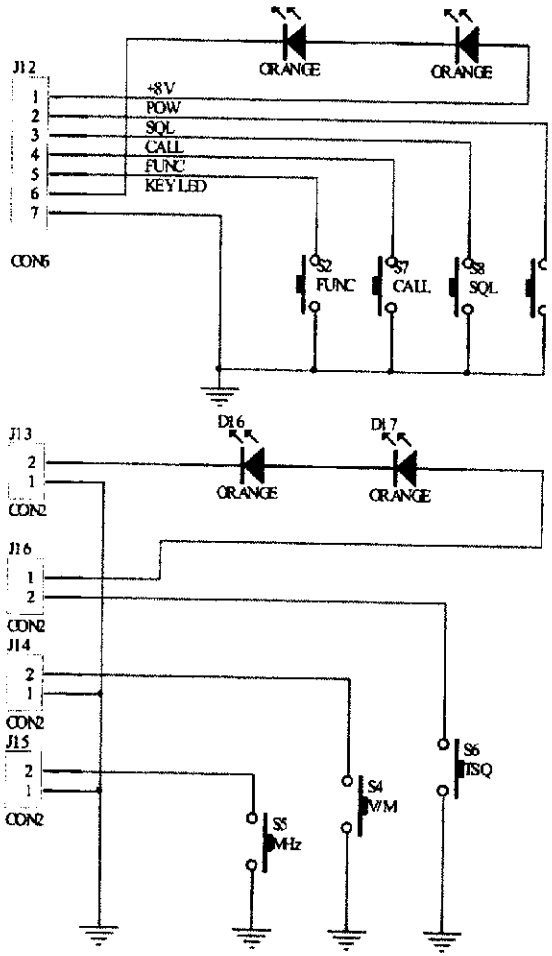

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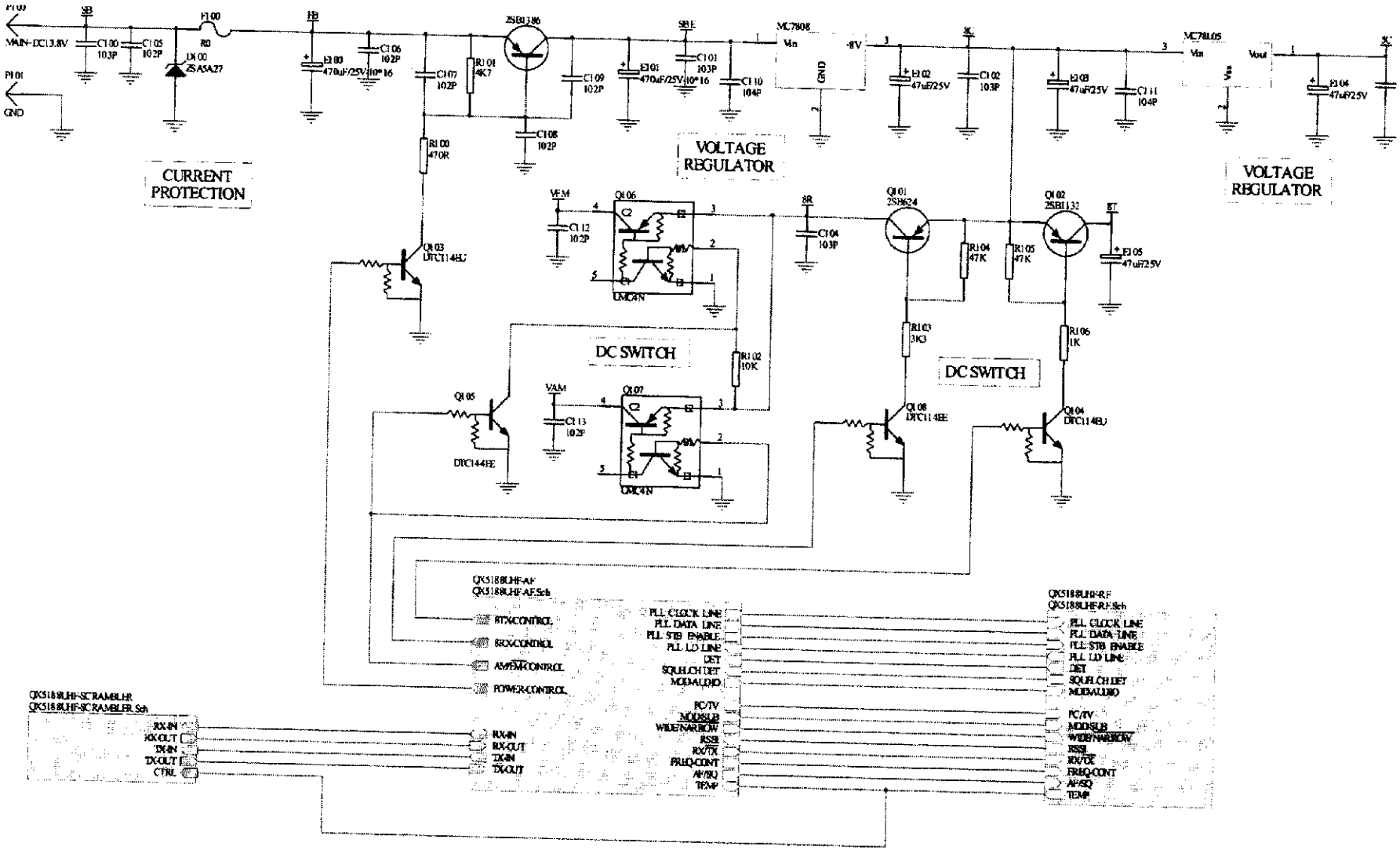

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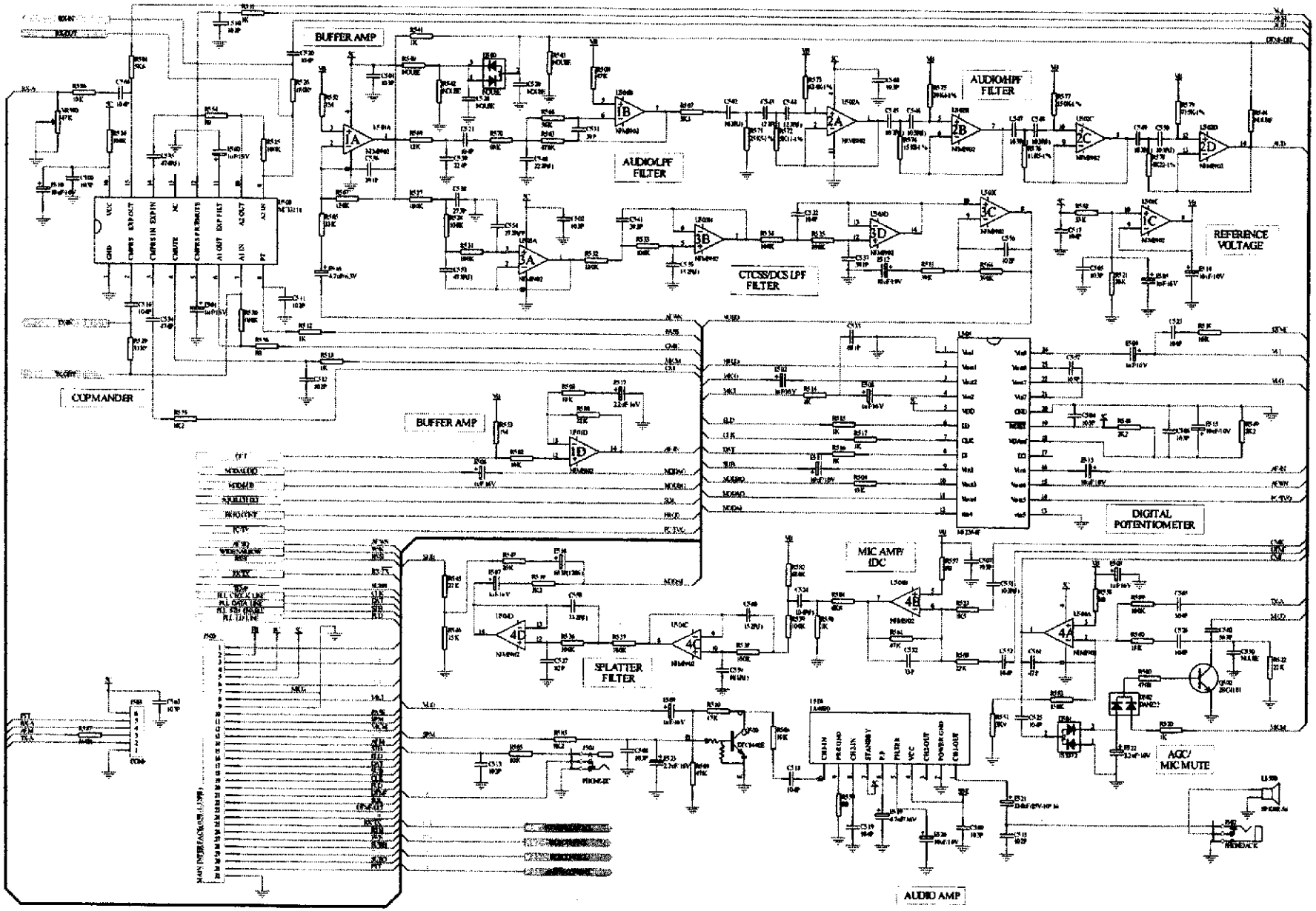

BLOCK DIAGRAM